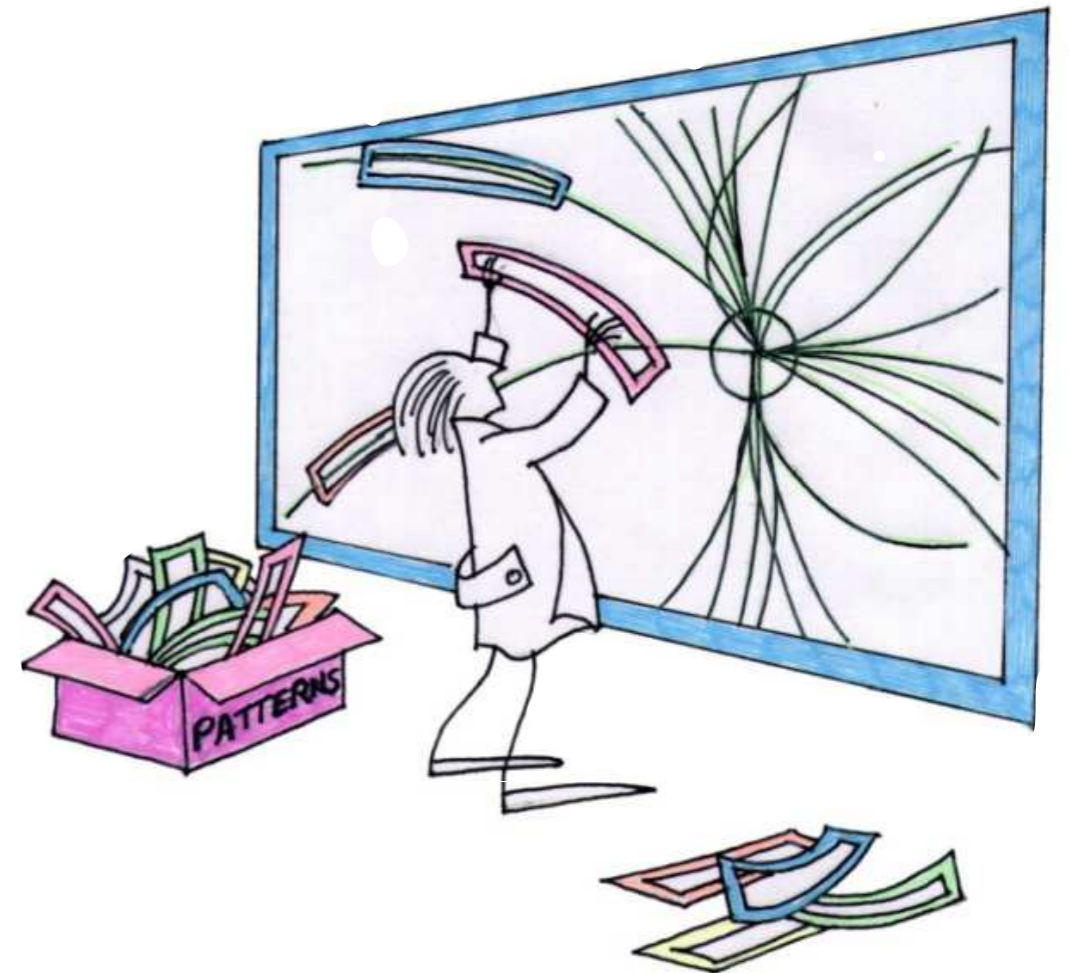


FTK: a Fast Track Trigger for ATLAS

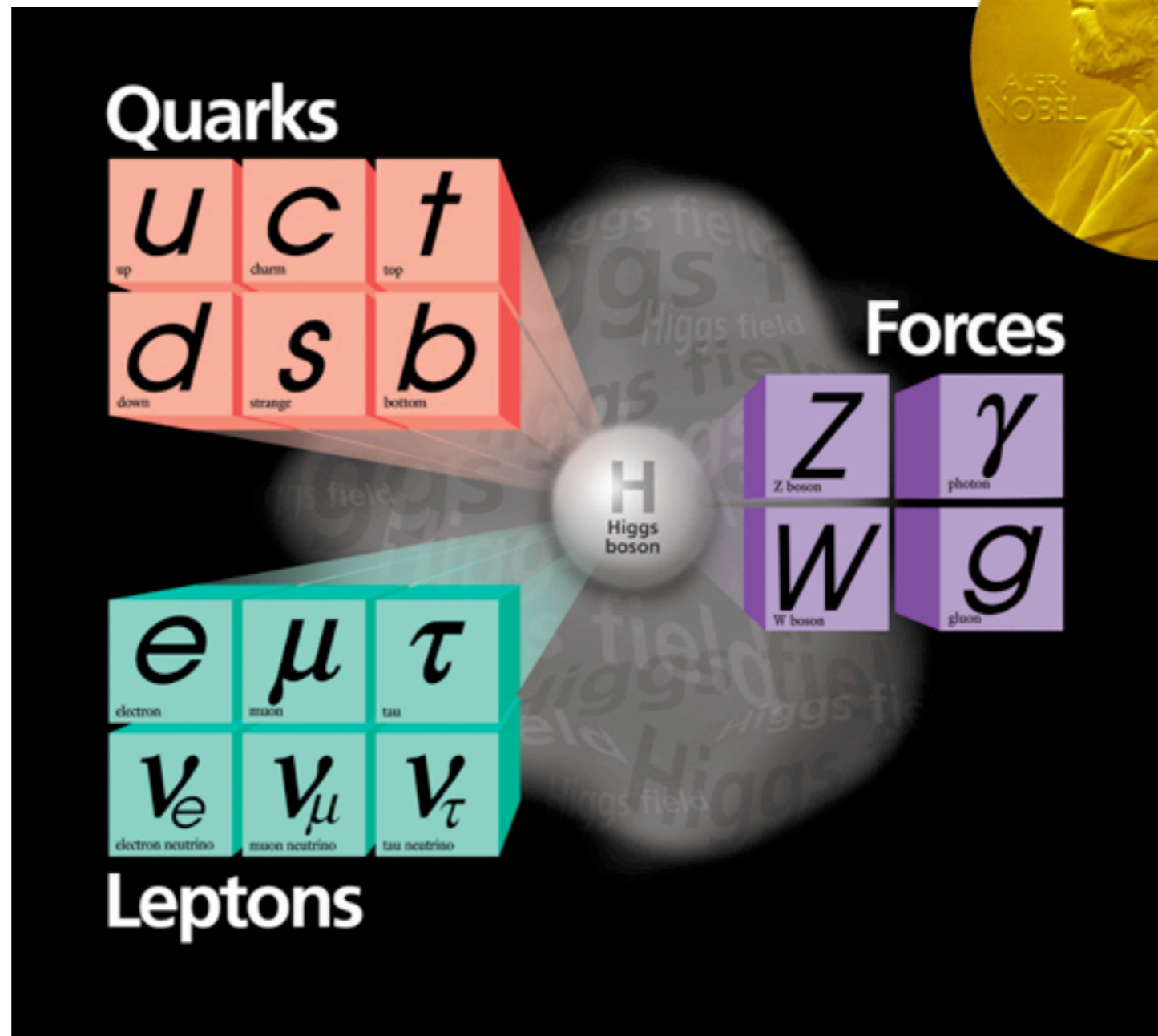
Lauren Tompkins



THE UNIVERSITY OF
CHICAGO

Lessons from Run I

- Triumphant discovery of a Higgs boson



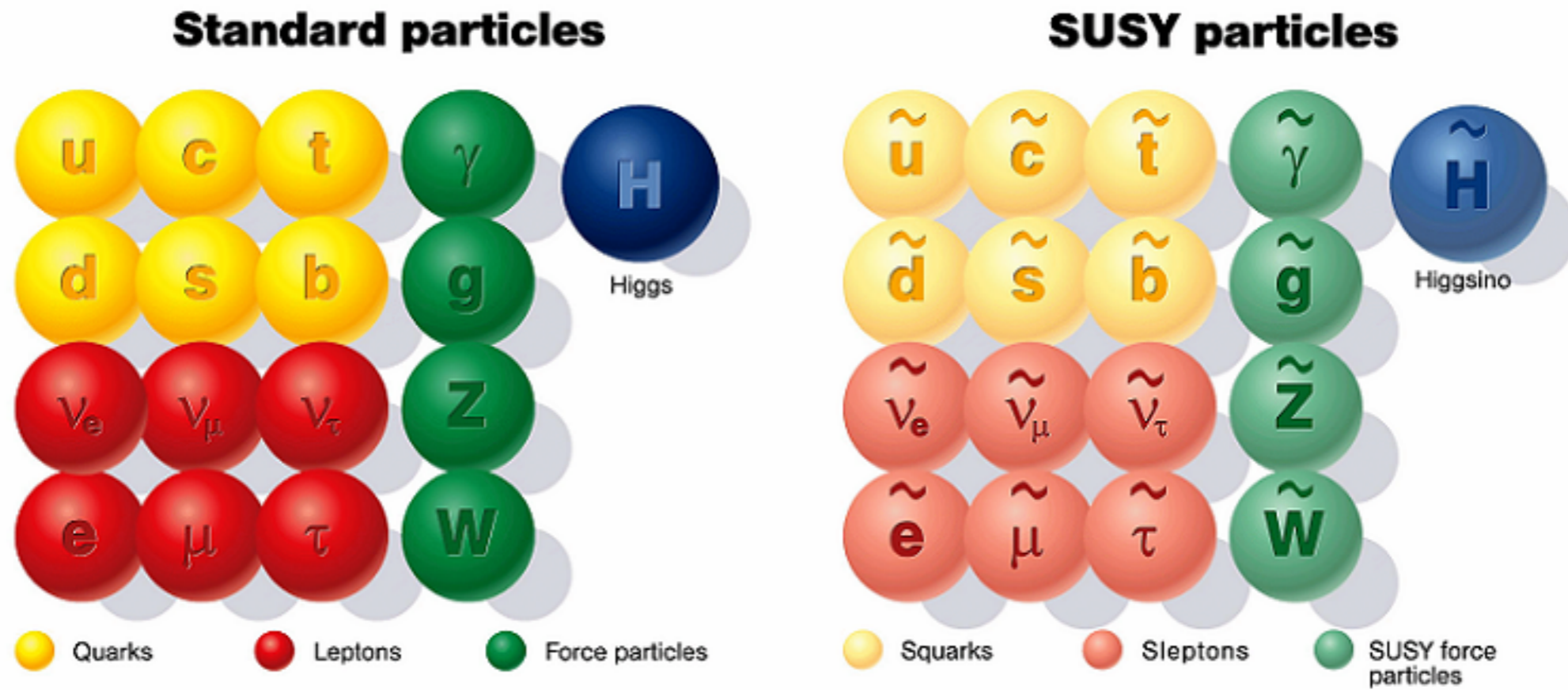
Lessons from Run I

- Nothing else!



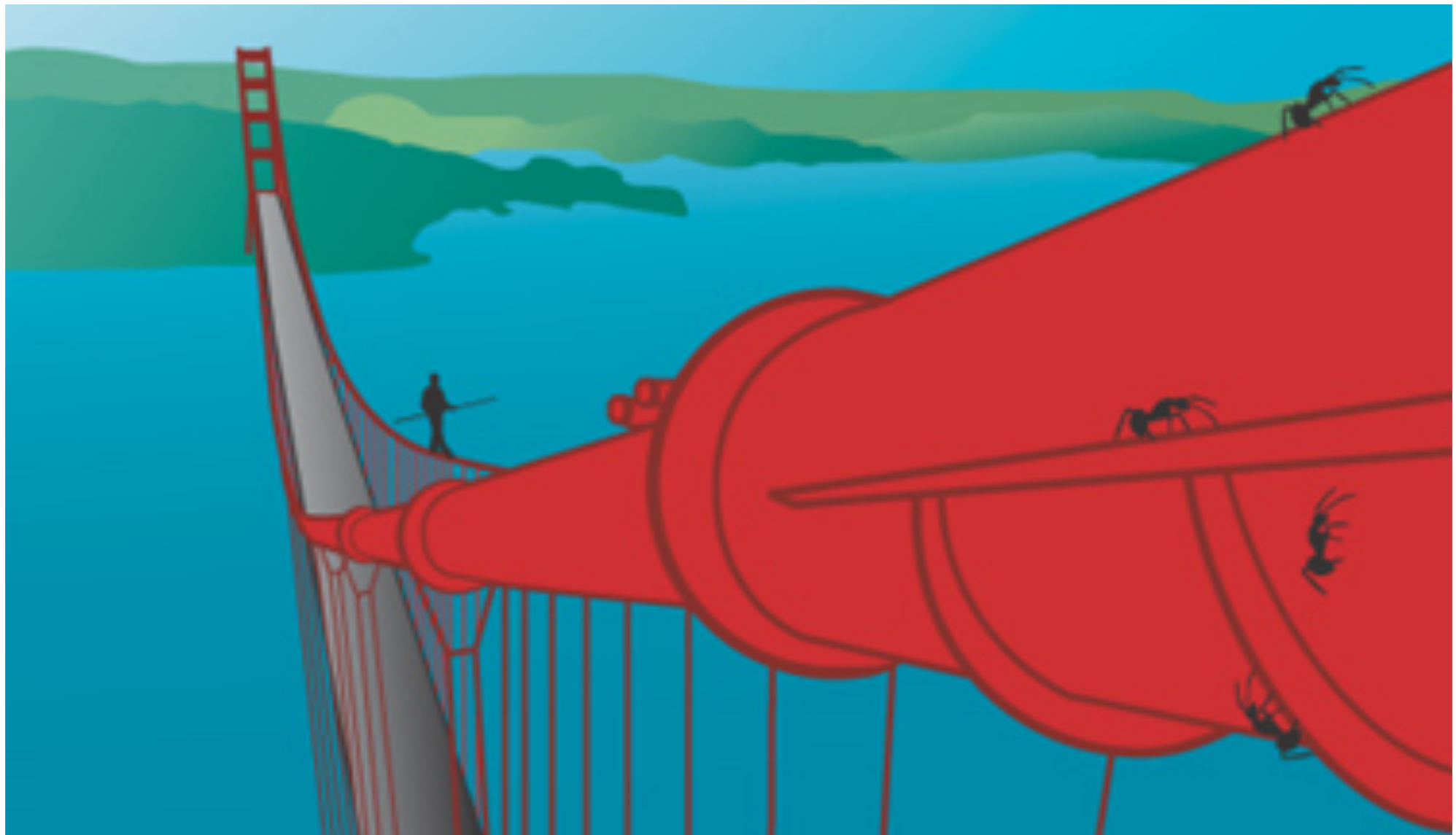
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Lessons from Run I

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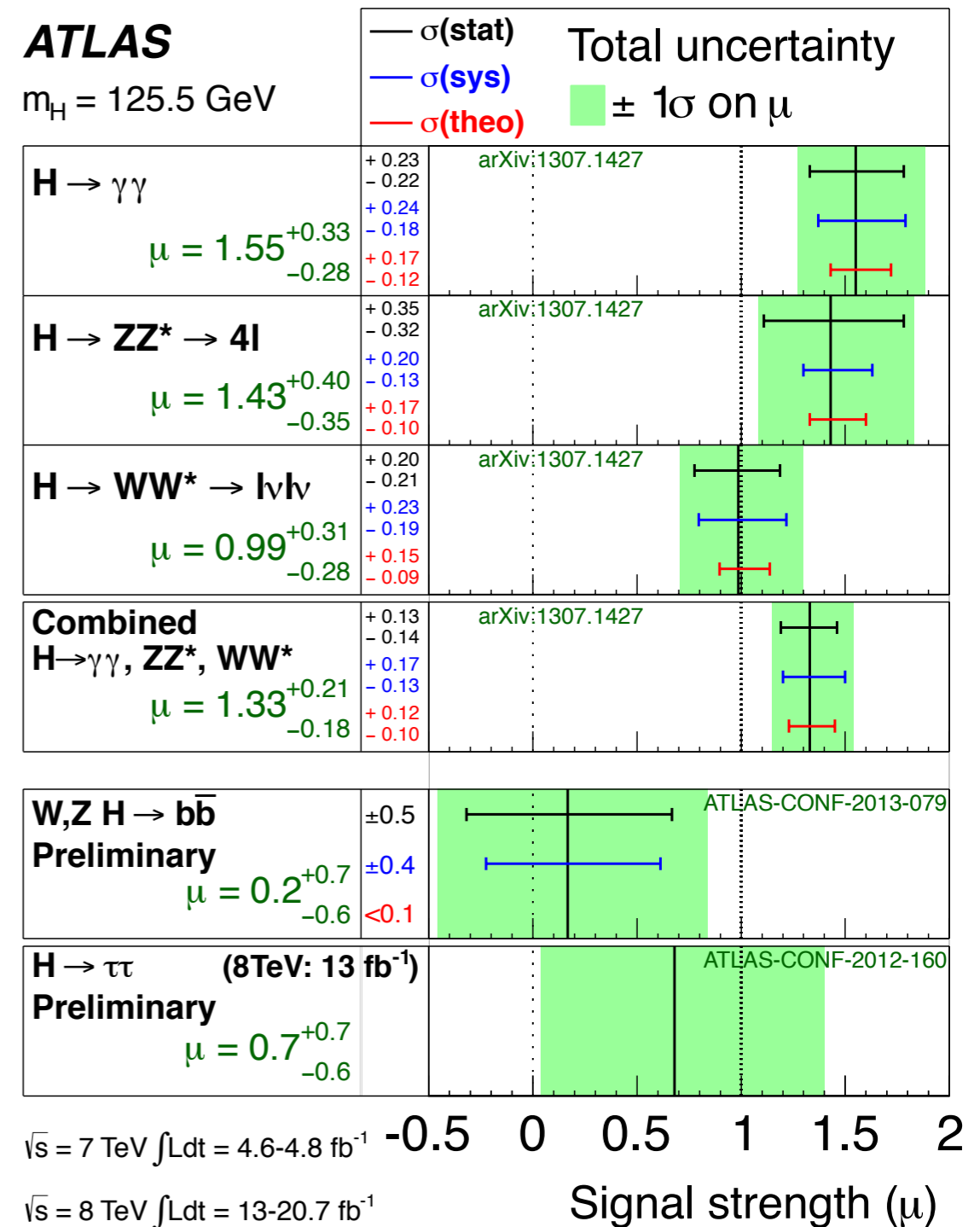
Lessons from Run I

- Nothing else!



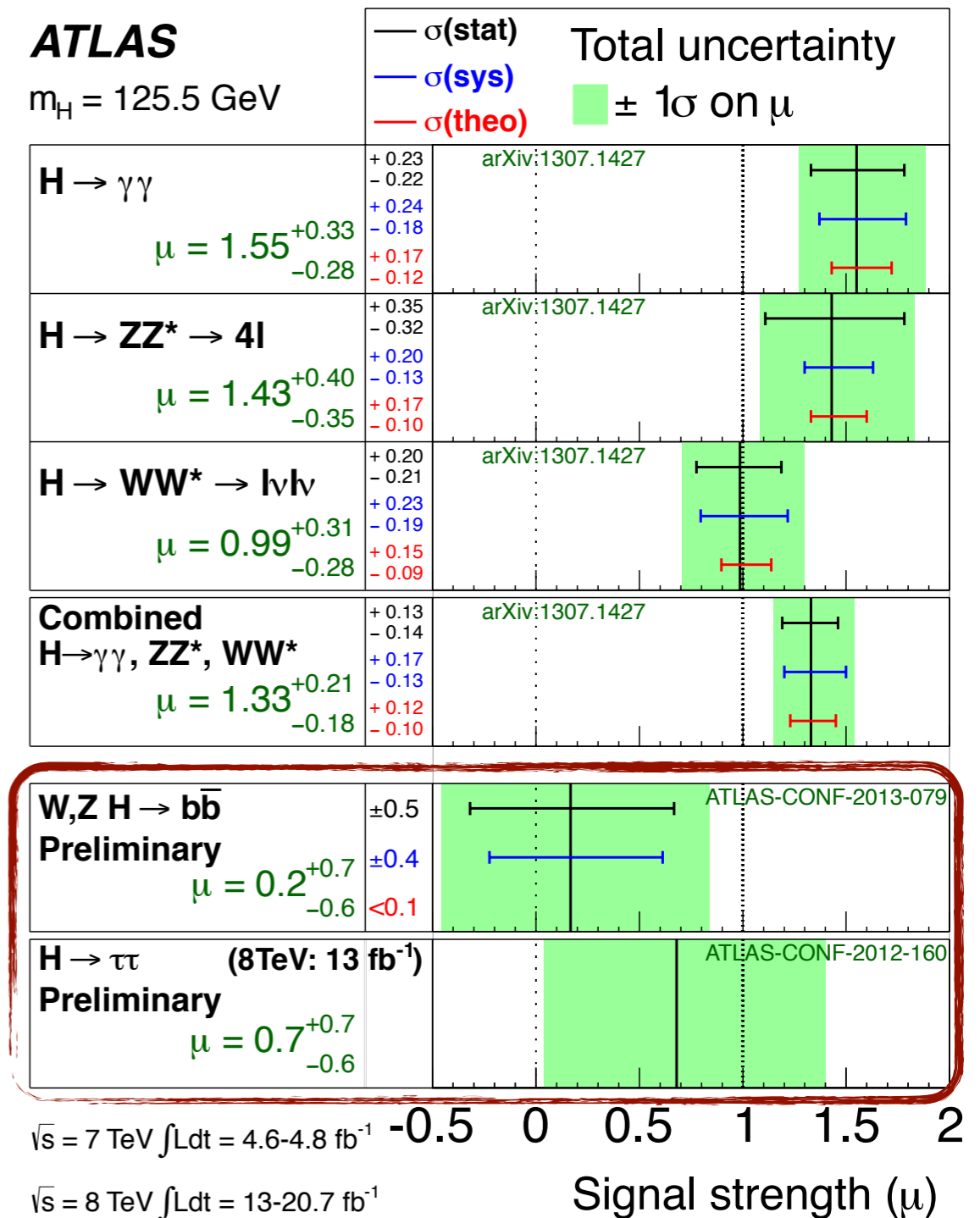
Looking to 2015 and beyond

- Measure the properties of the new boson
 - b and tau measurements critical!
- Search wider, farther and deeper for new physics
 - Stop, sbottom and stau searches have weakest limits
 - Must keep flexibility for more exotic signatures, e.g. resonances decaying to many heavy qs
- Heavy fermions may be key to this program



Looking to 2015 and beyond

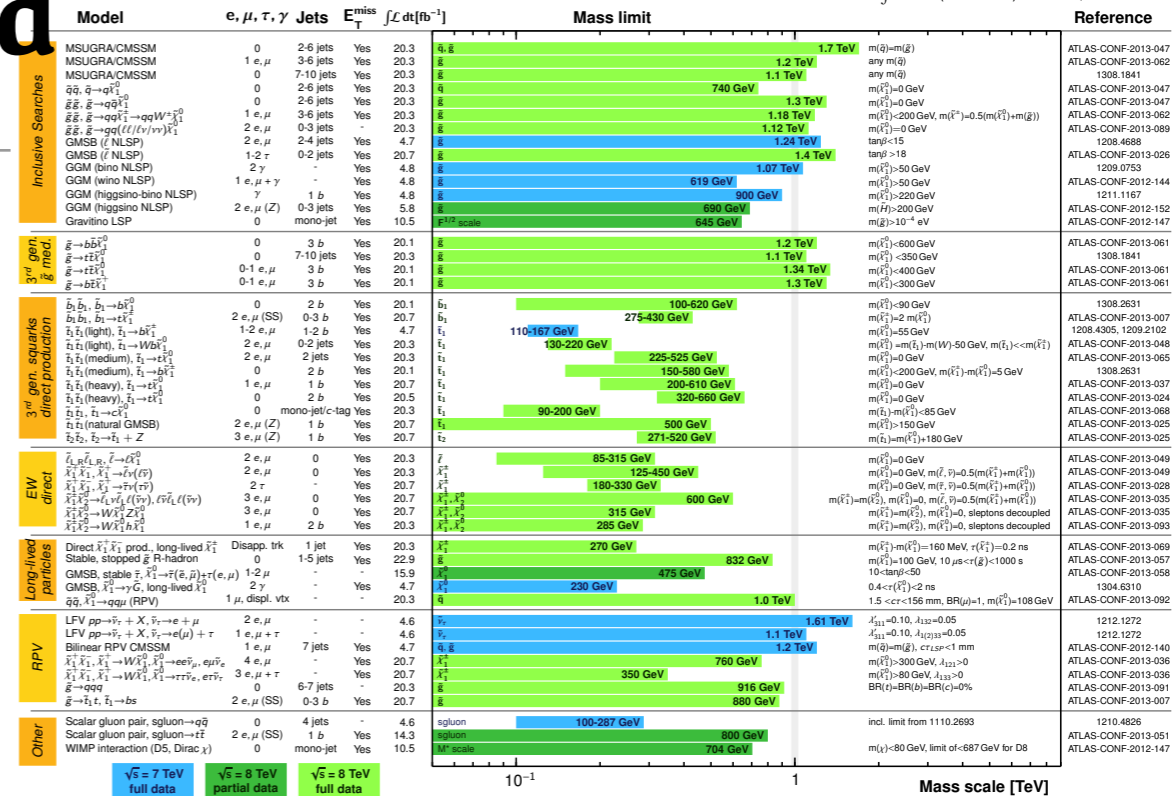
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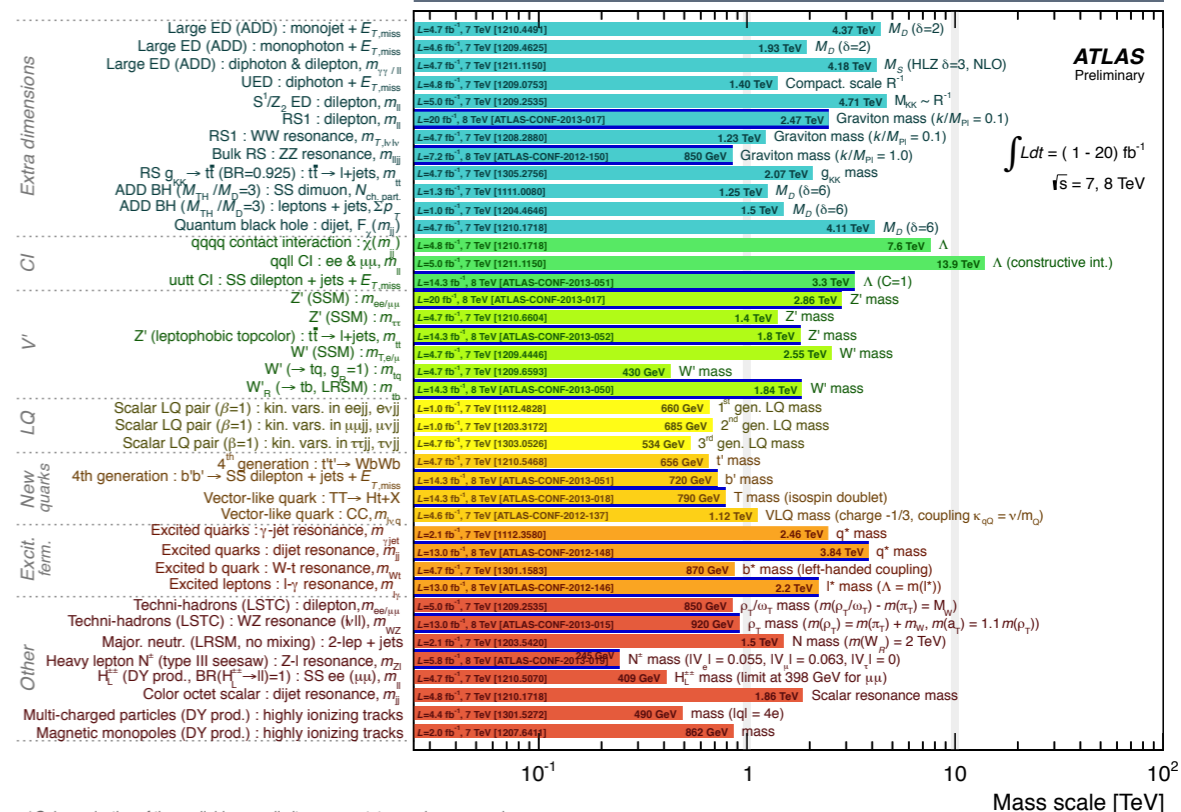
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ATLAS SUSY Searches* - 95% CL Lower Limits
Status: SUSY 2013

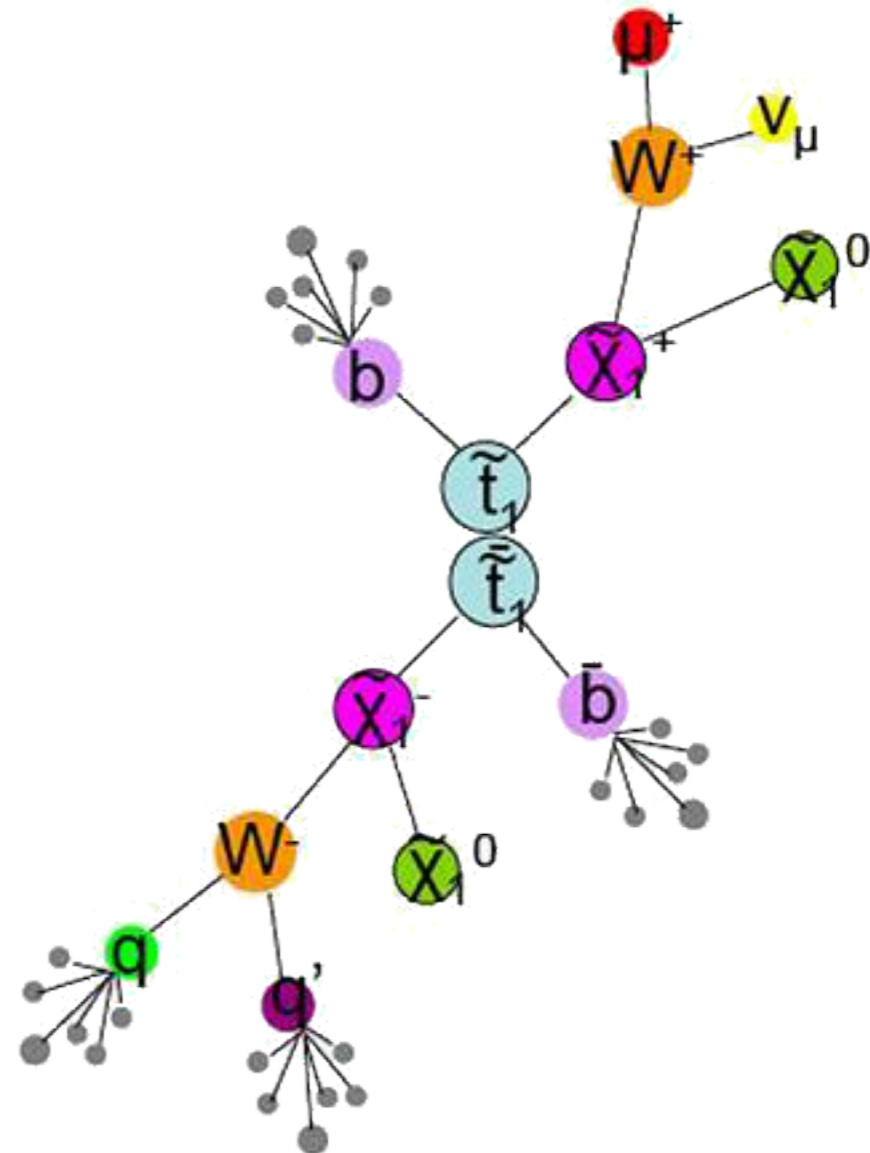


ATLAS Exotics Searches* - 95% CL Lower Limits (Status: May 2013)



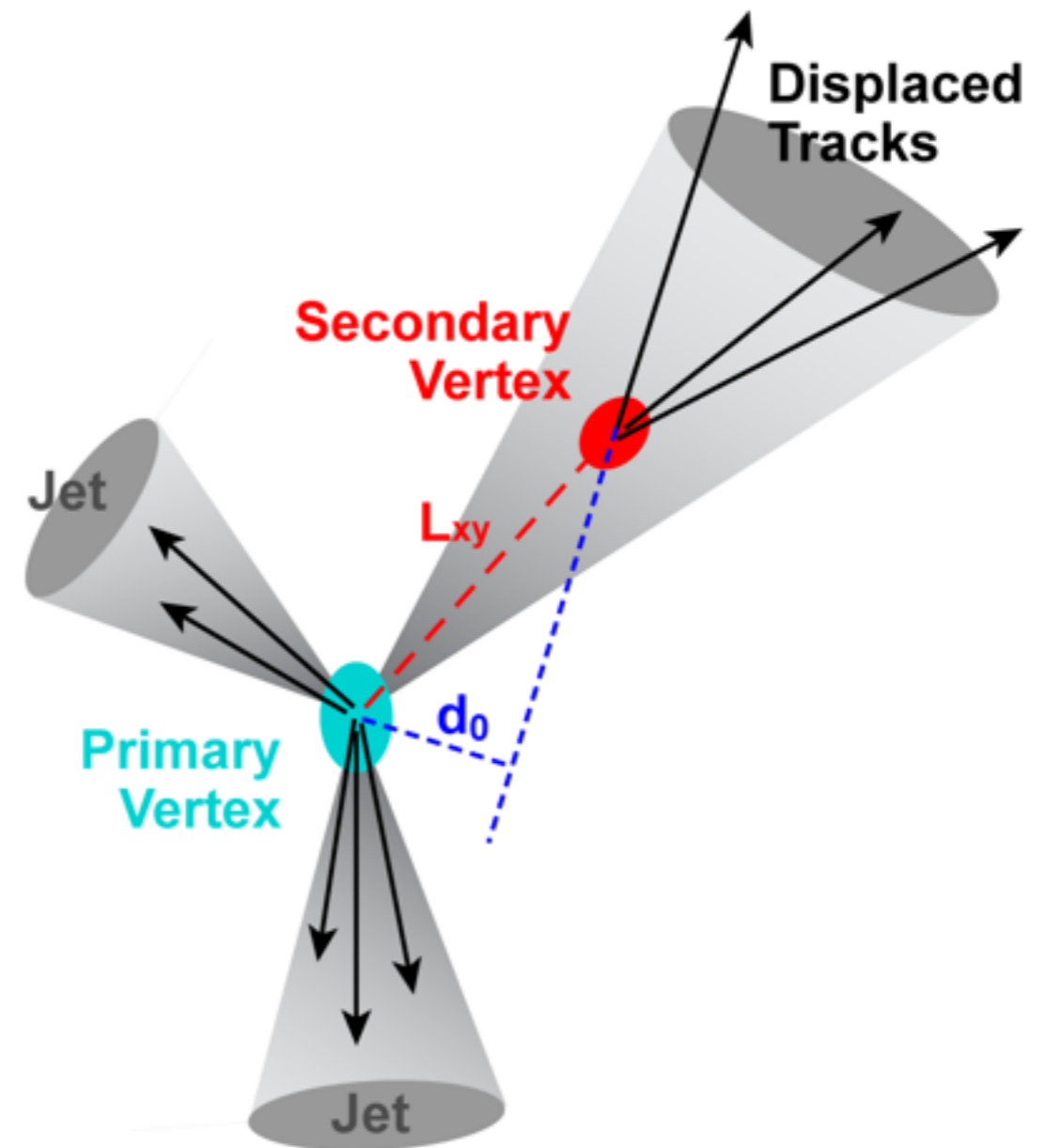
Carrying out the Physics Program

- Need to be able to identify:
 - 3rd generation particles:
 - taus, b-quarks
 - Displaced vertices from B-hadron decays
 - 1- and 3-prong tau decays
 - Leptons from electroweak decays:
 - Isolated electrons and muons
 - Jets and Missing Energy
 - Tracking is critical!



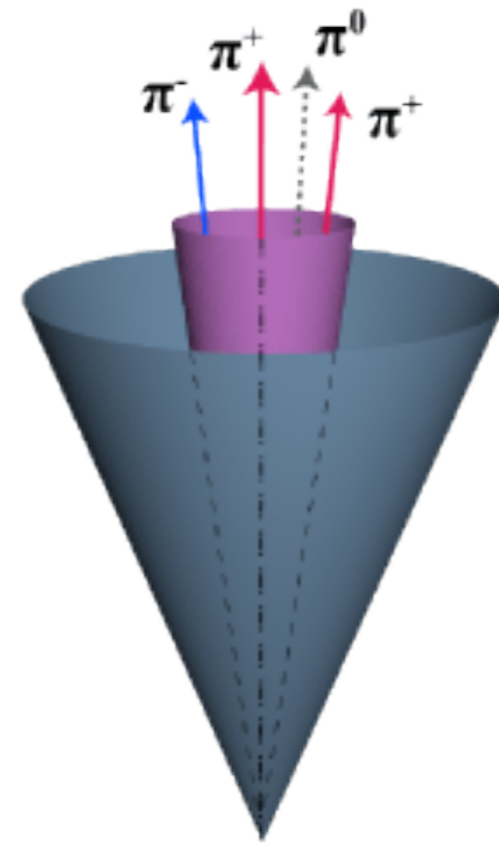
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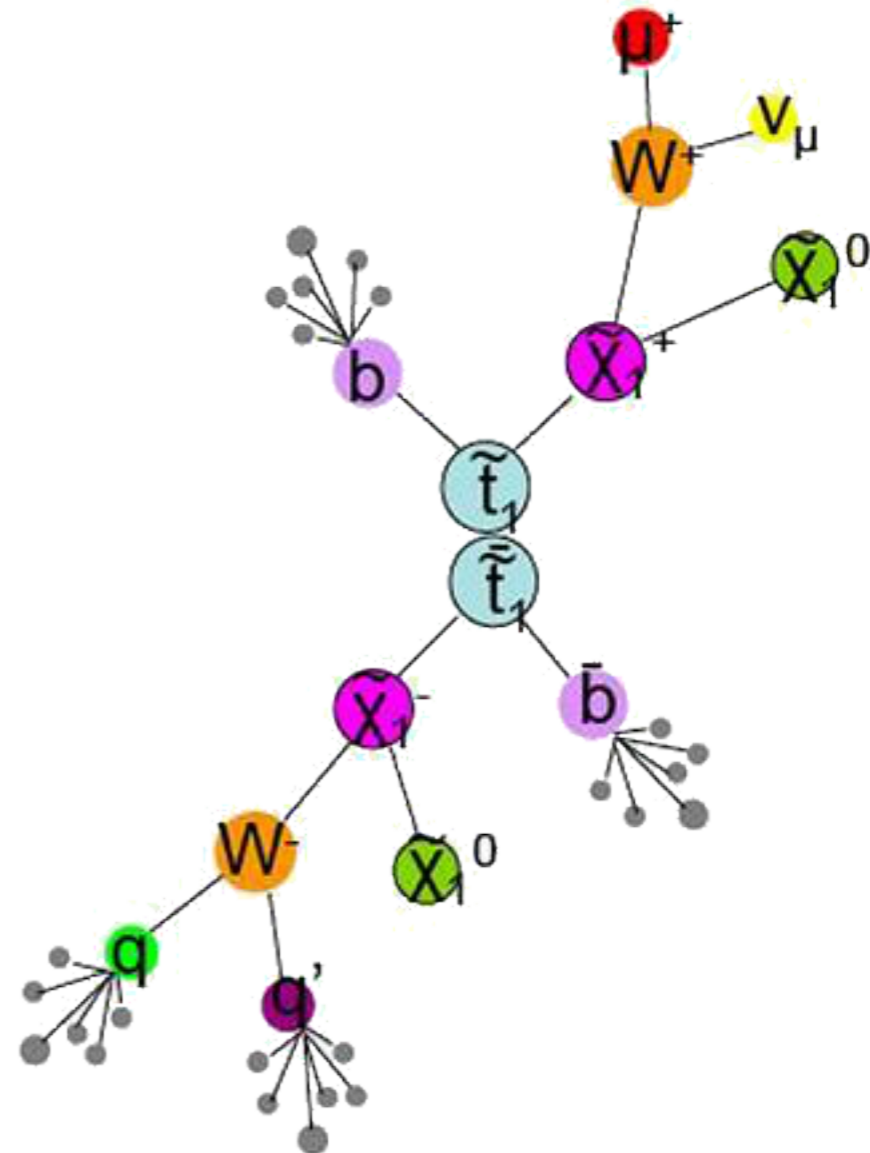
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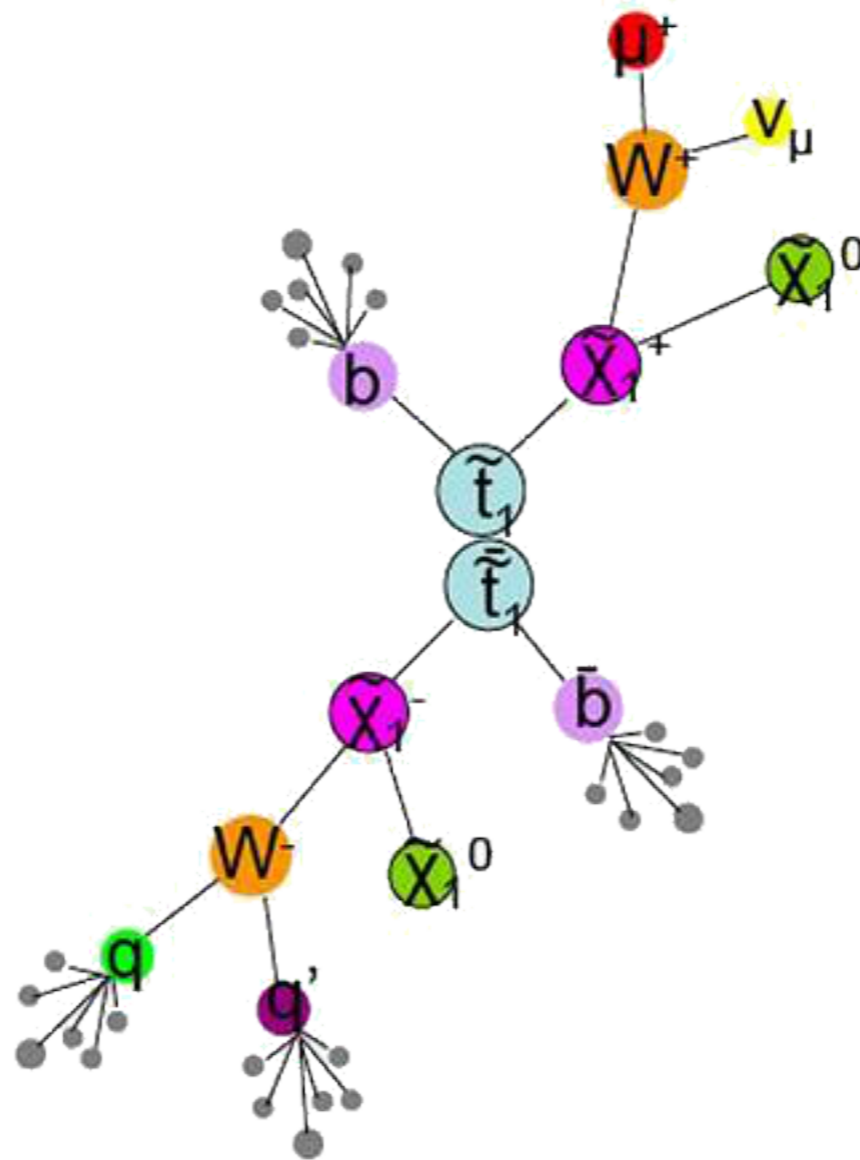


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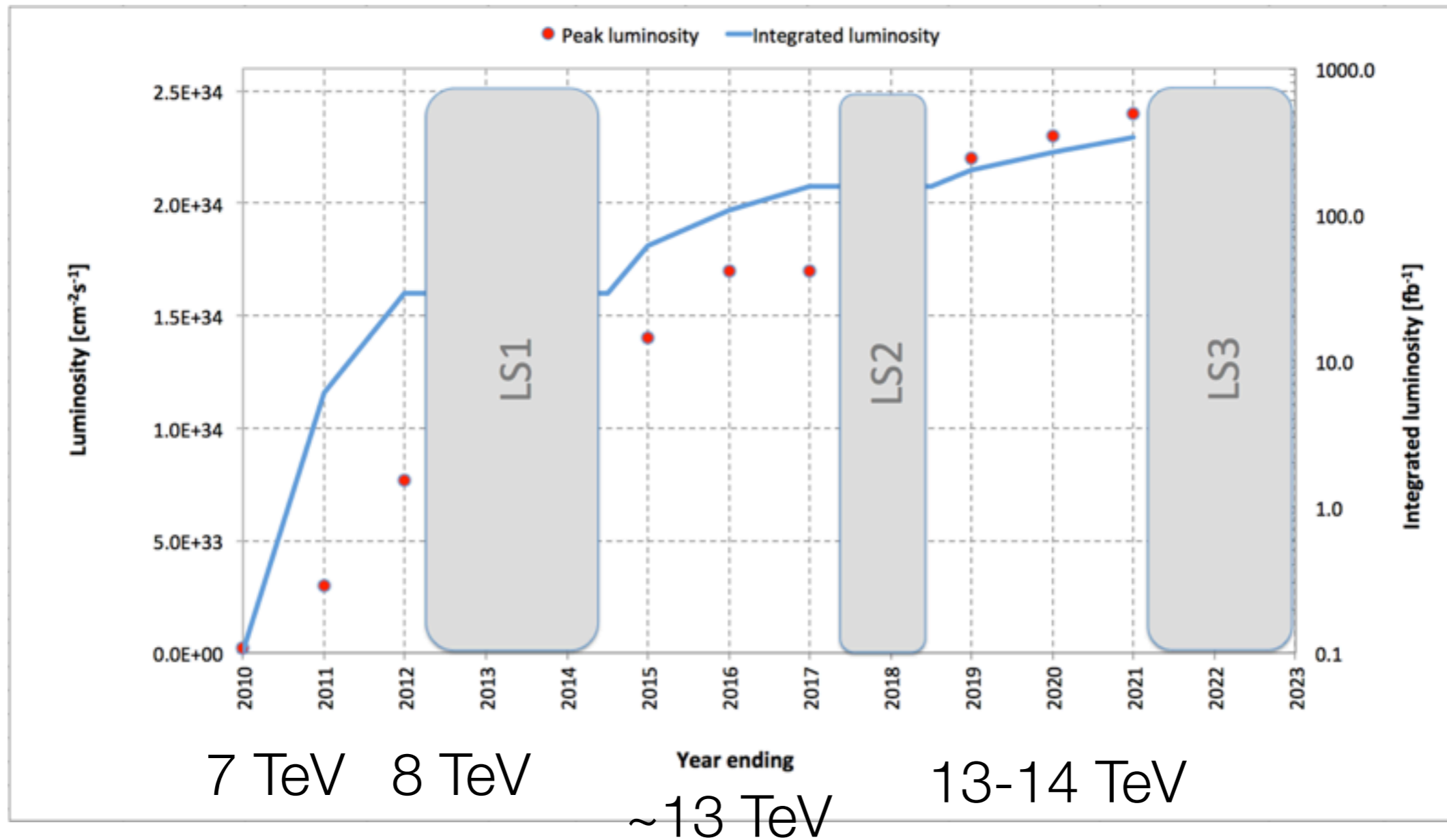
The challenge



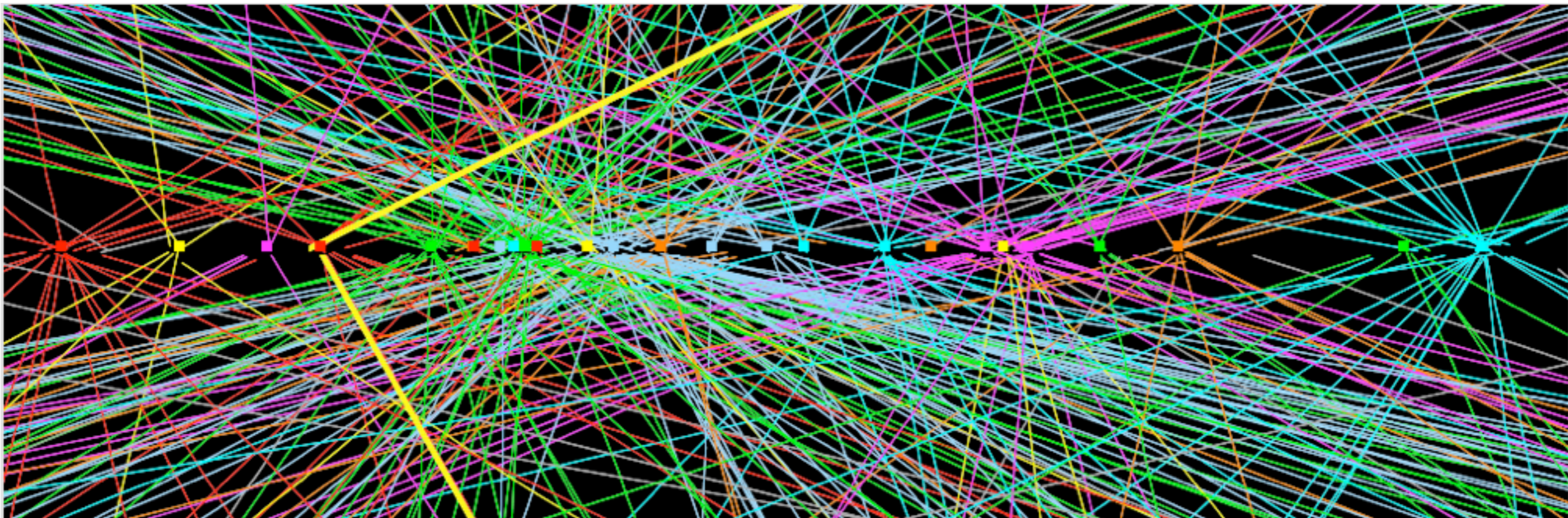
The challenge



Run II and III conditions

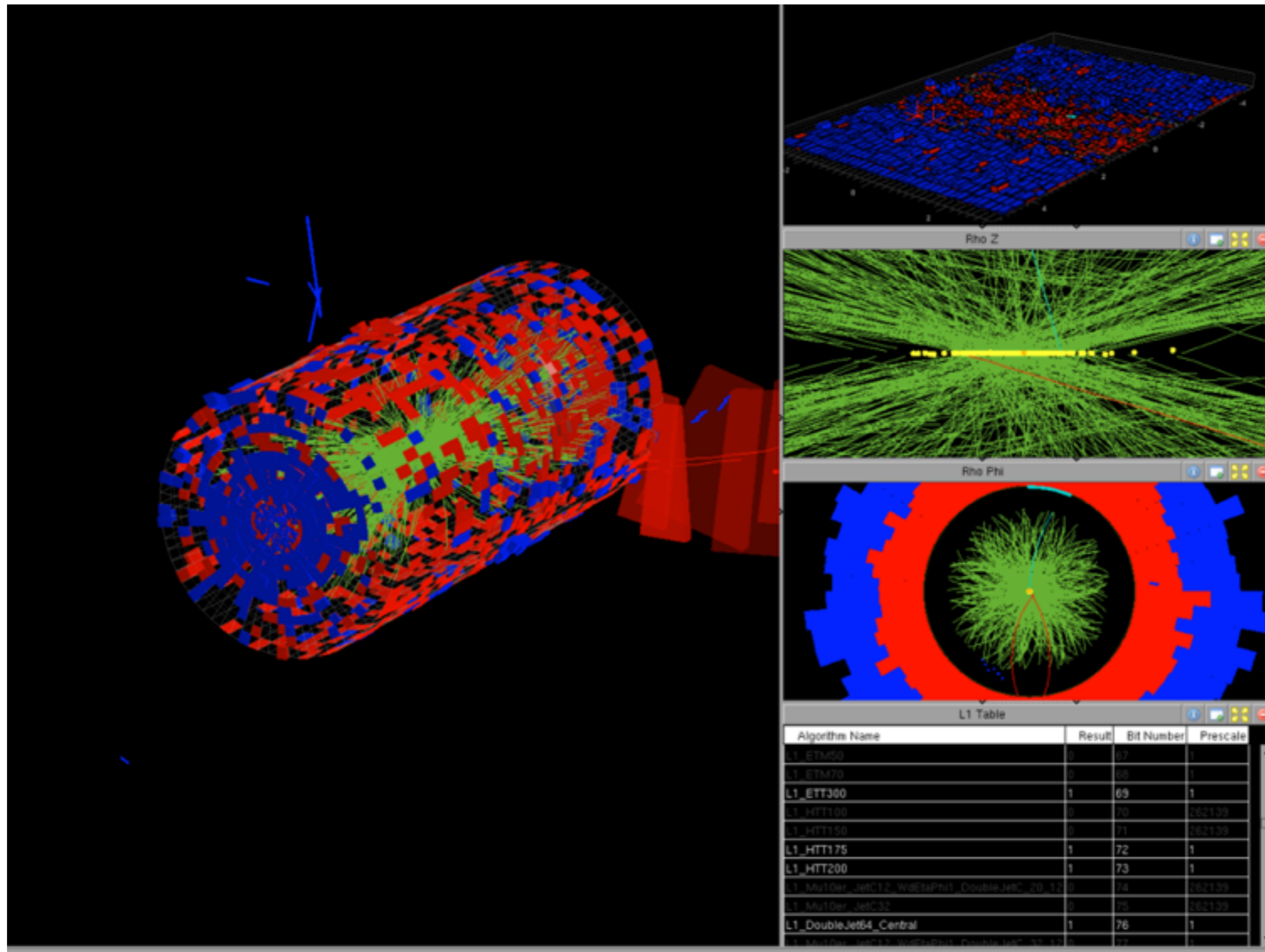


Challenges



April 15th 2012, 25 reconstructed vertices, $Z \rightarrow \mu\mu$ candidate event

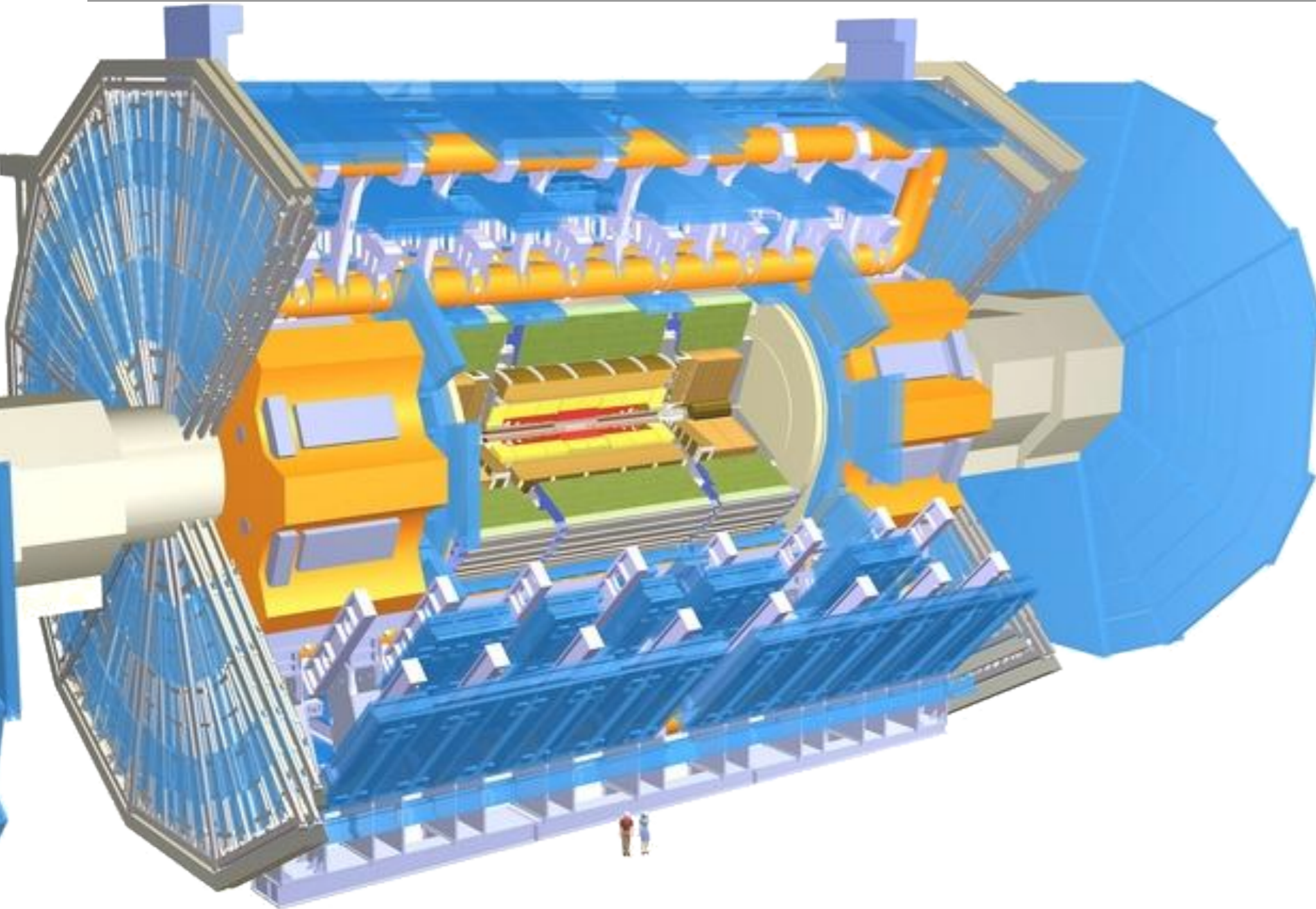
Challenges



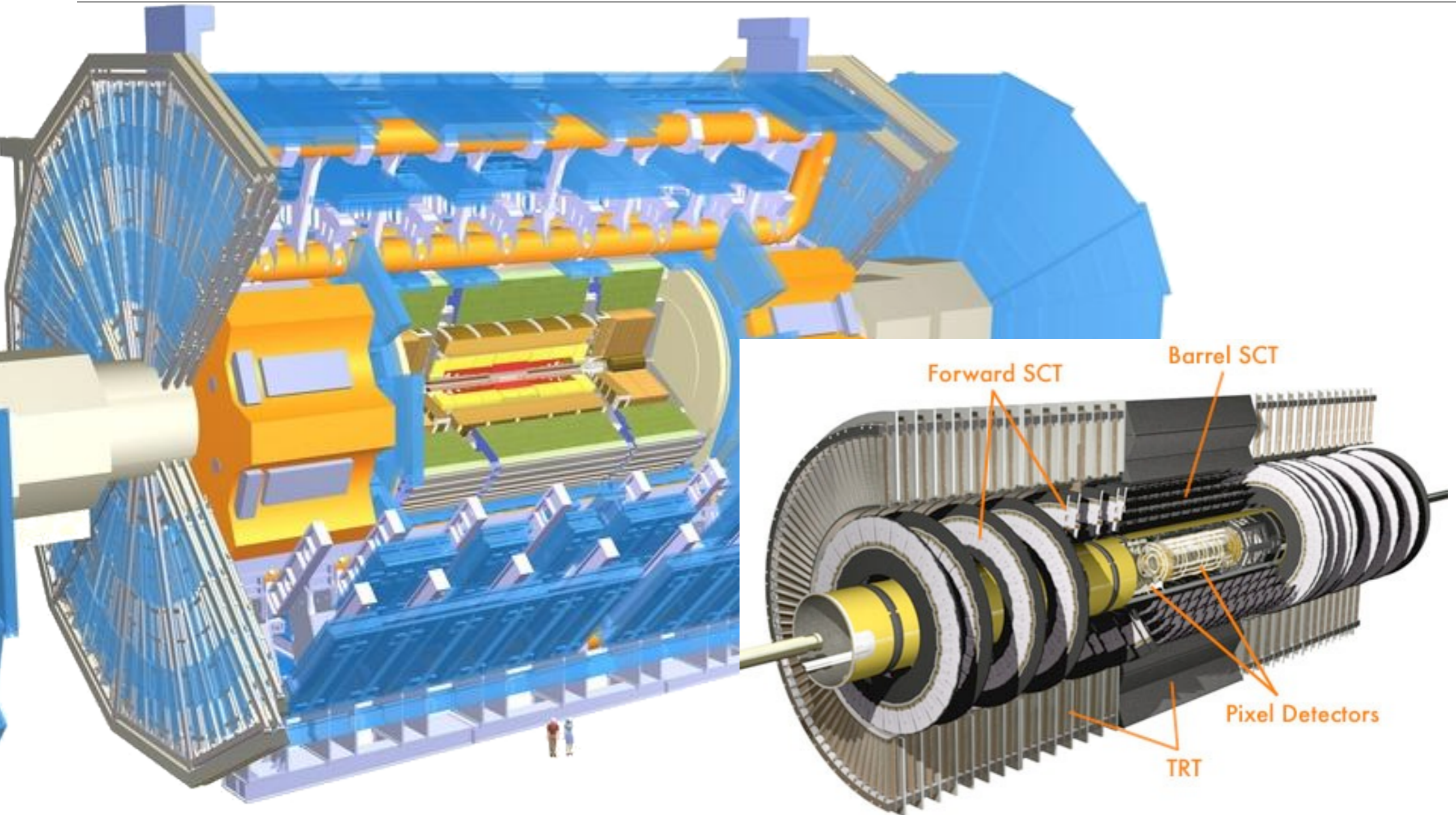
CMS, 78 reconstructed vertices



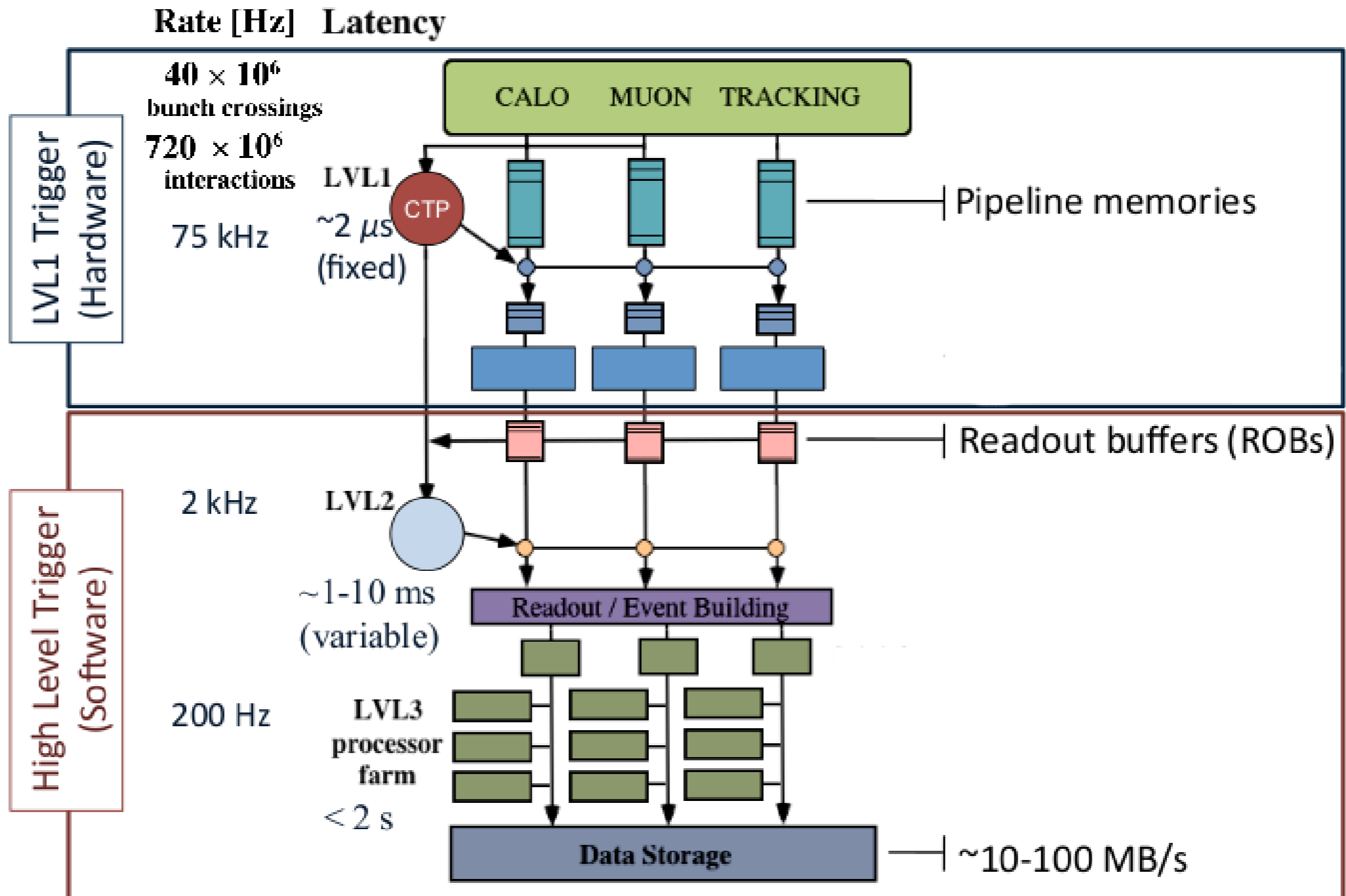
ATLAS



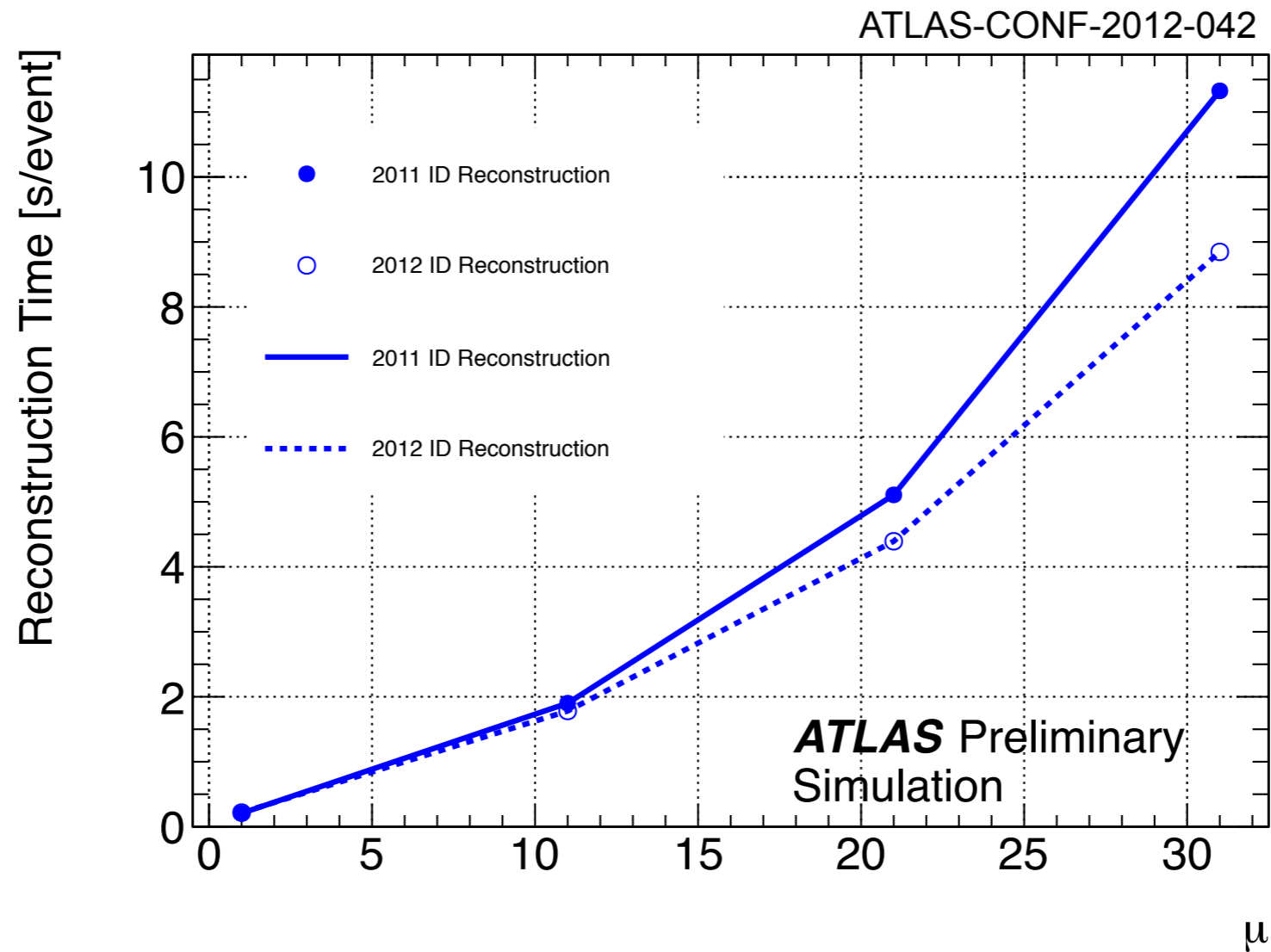
ATLAS



ATLAS Trigger System



Tracking at High Lumi is Tricky



- Huge combinatorial problem, very non linear with number of interactions
 - Use algorithms in software run on CPUs: slow!
- FTK solves these problems with a hardware based approach
 - Full detector reconstruction in less than 100 microseconds

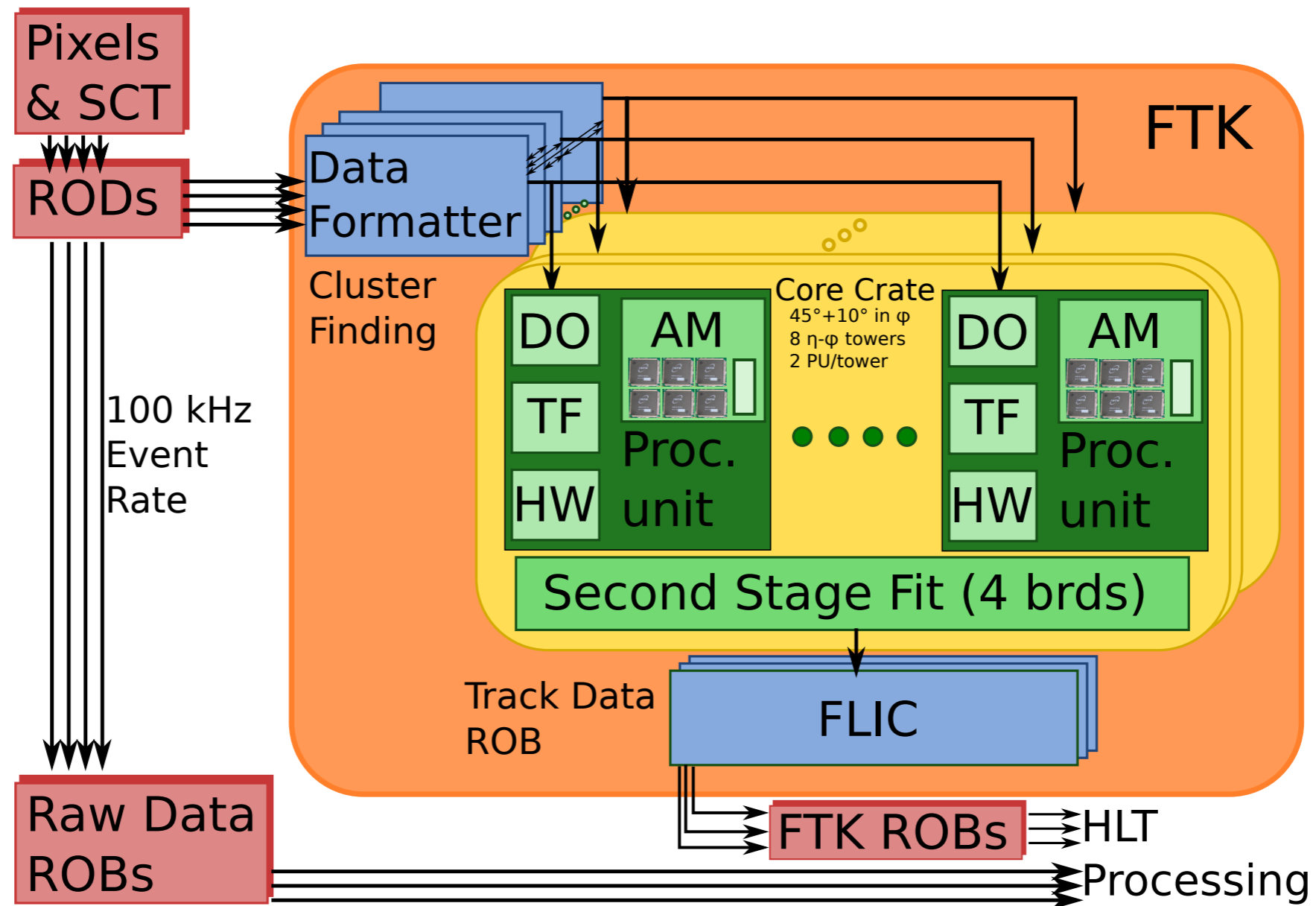


Conceptual Design

- Divide the detector η - ϕ towers: **Parallelize** the problem
- Convert clusters into coarse resolution hits: **Reduce** the data volume
- Compare hits to many pre-stored track patterns simultaneously: **Eliminate** costly loops
- Use a linearized fit for track candidates: **Simplify** algorithms
- All implemented in FPGAs or custom ASICs: **Hardware** solution



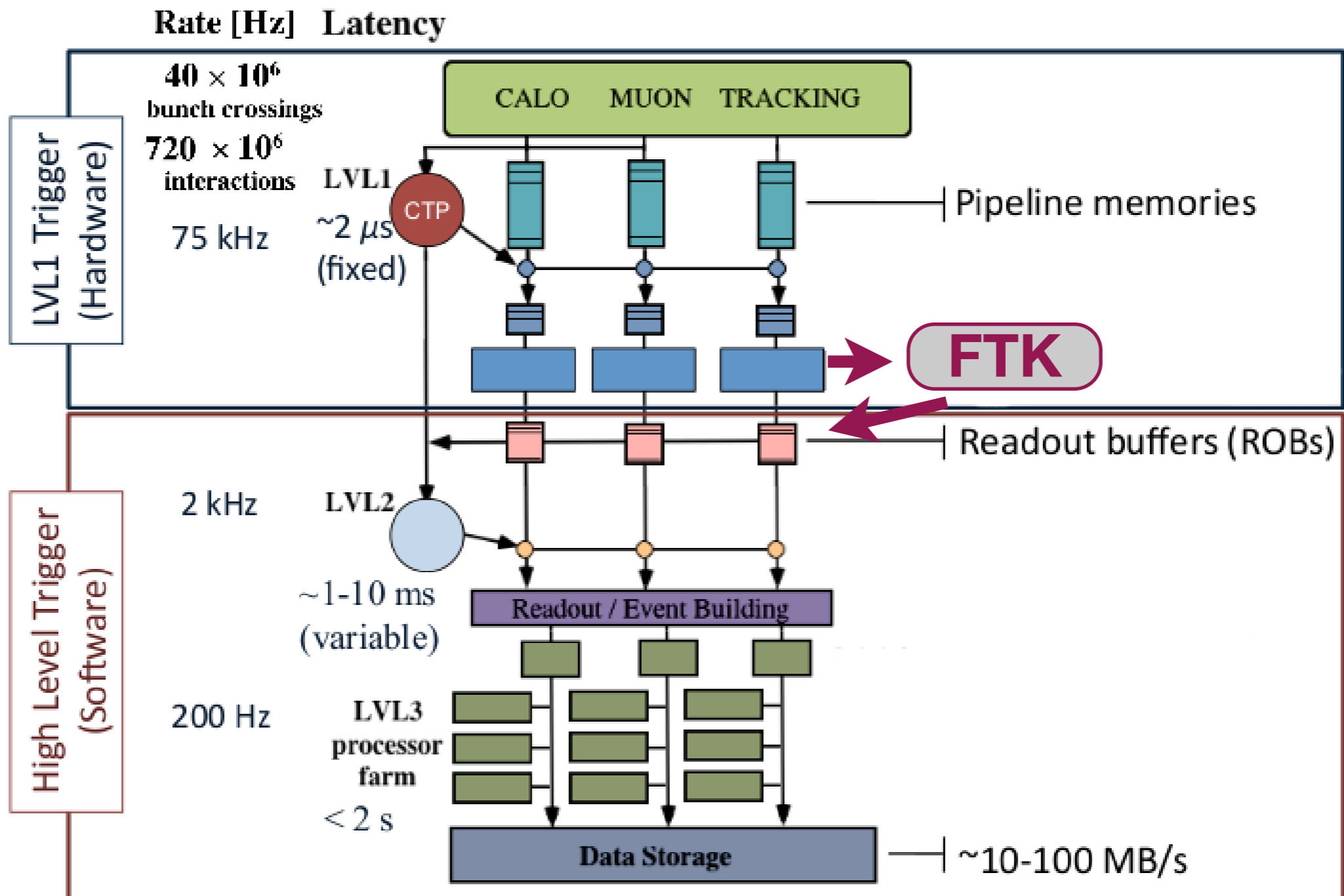
System Architecture



64 η - ϕ towers contained in 8 core crates

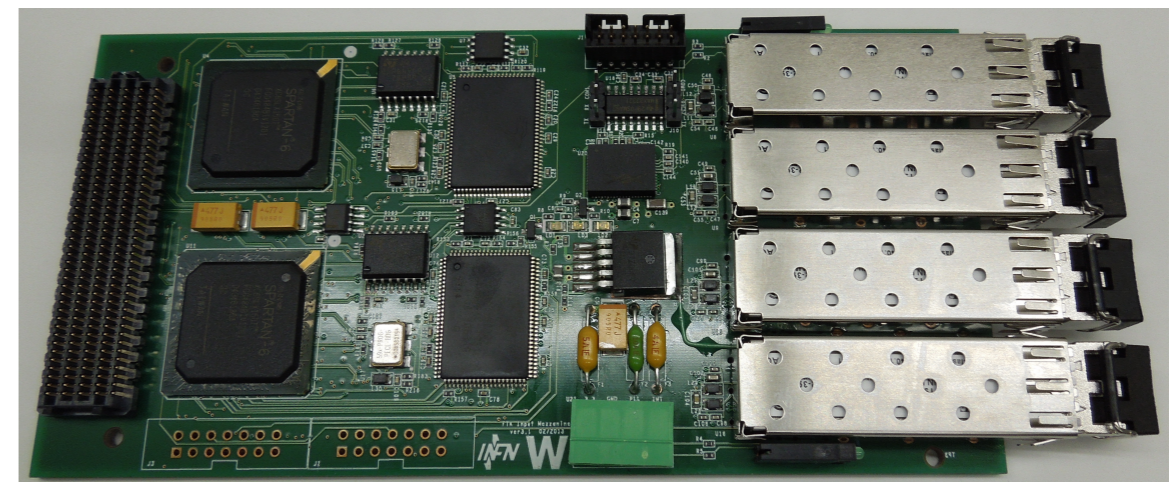
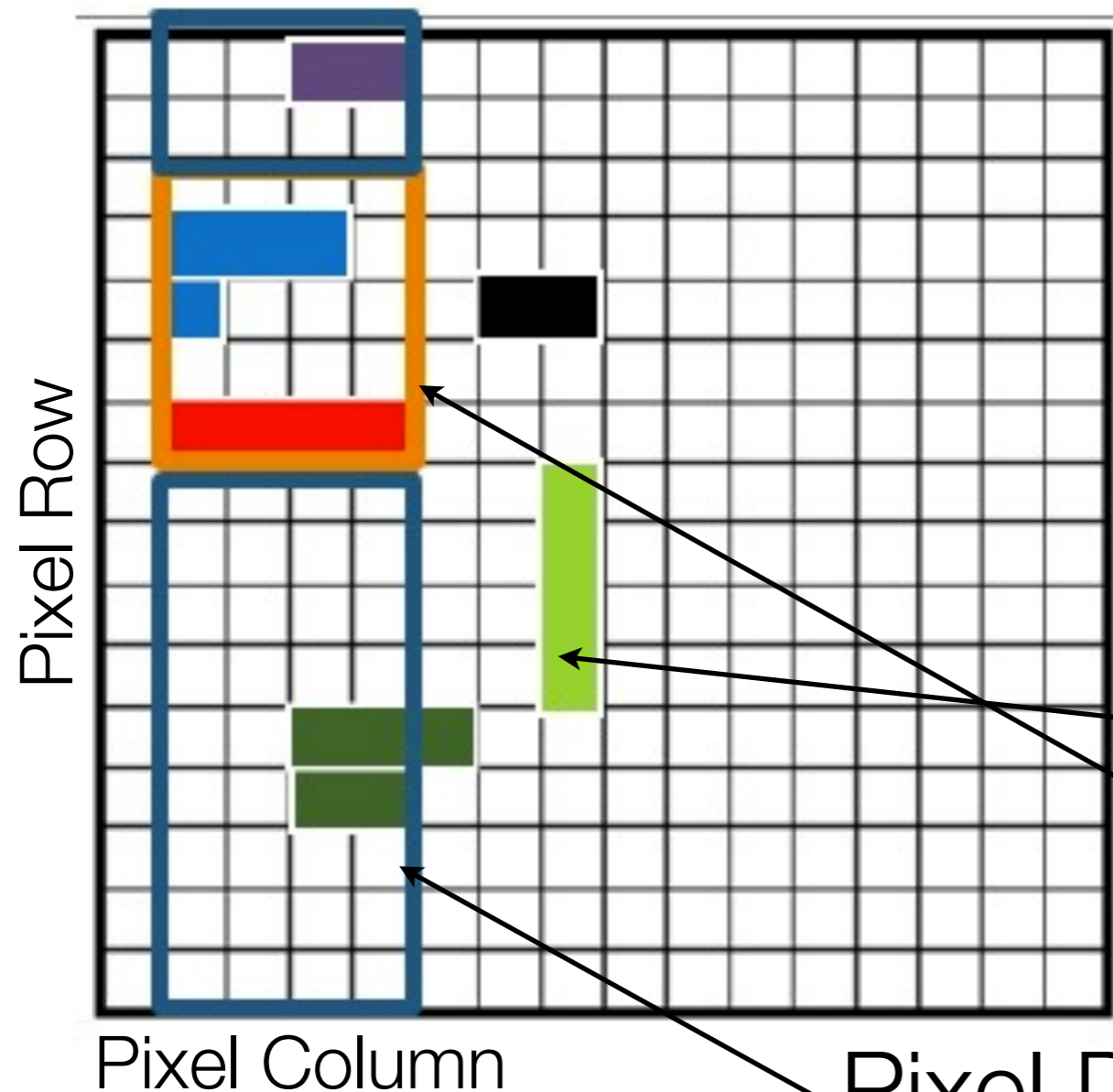


FTK in the ATLAS Trigger System



Stage 1: Clustering

- Receive data from silicon detectors
- Cluster pixel hits using sliding window algorithm in FPGA
- FPGAs on clustering mezzanines on Data Formatter boards

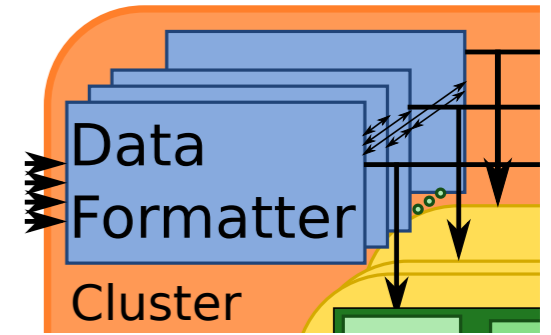


Clusters

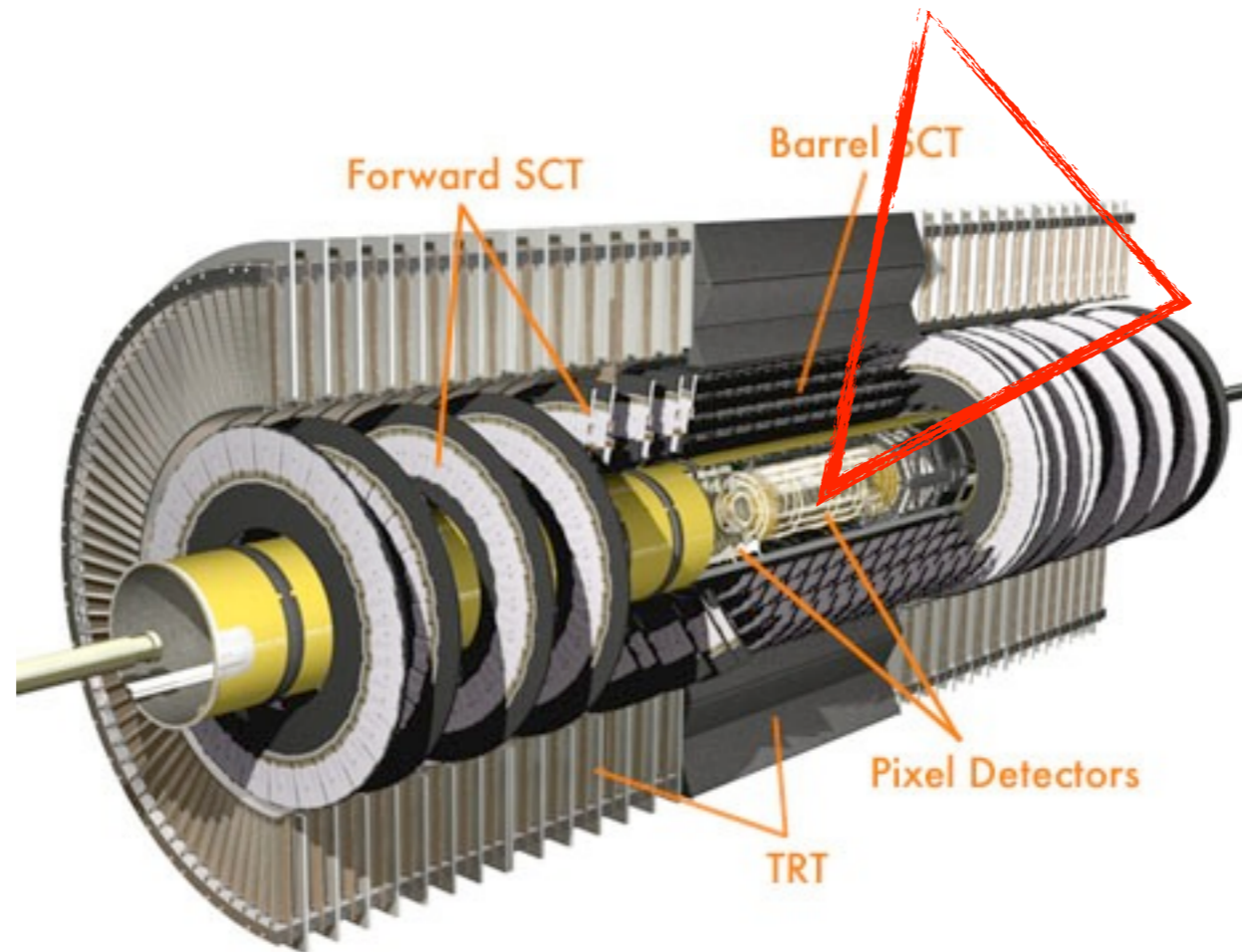
Sliding window

Pixel Data Buffer

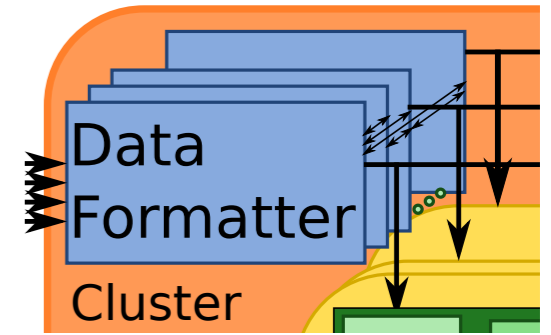
Stage 1: Data Formatting



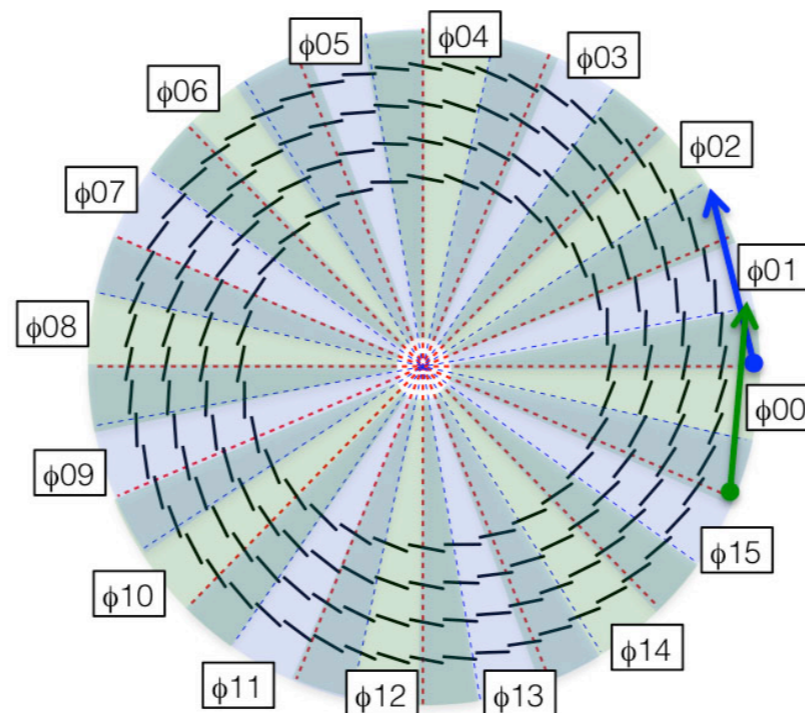
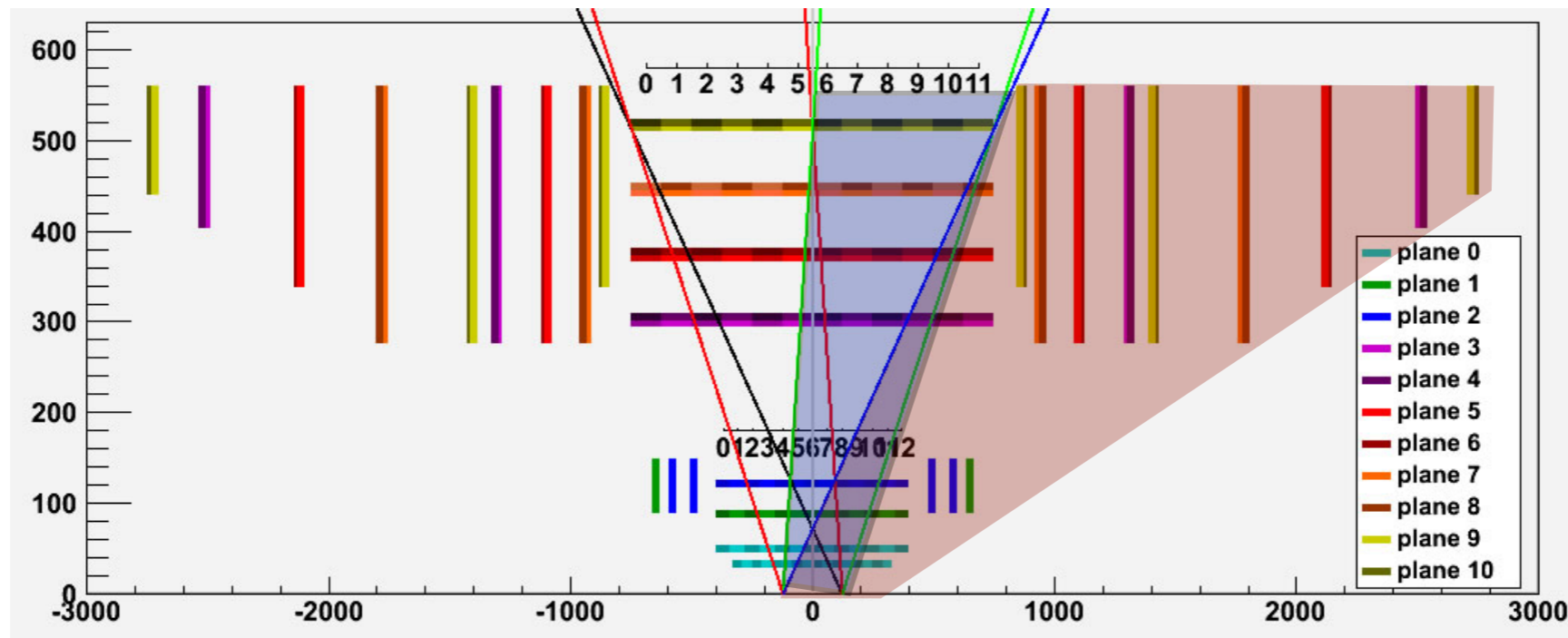
- Route clusters to FTK eta-phi towers



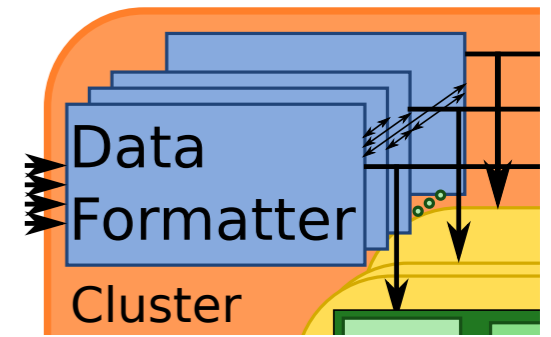
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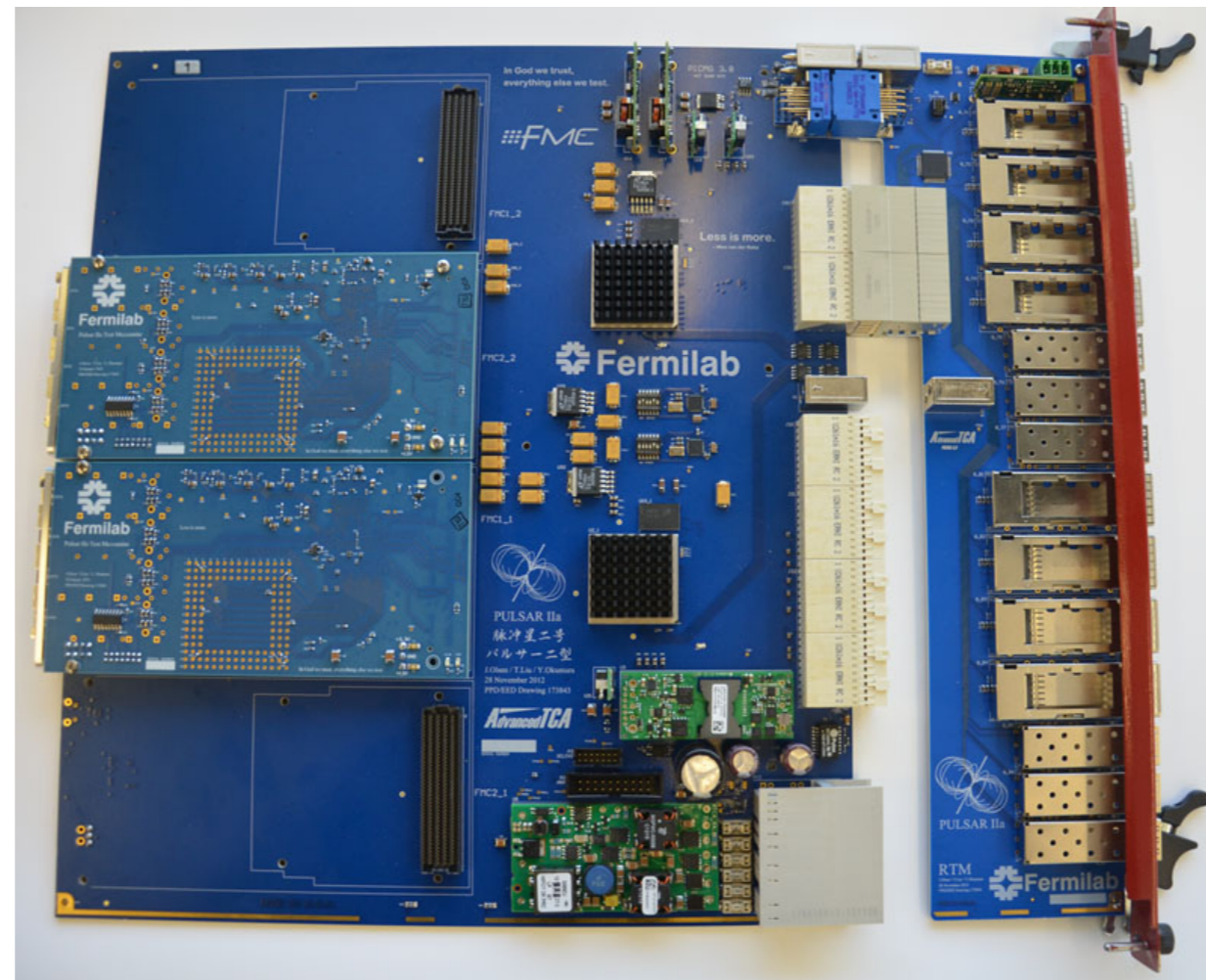
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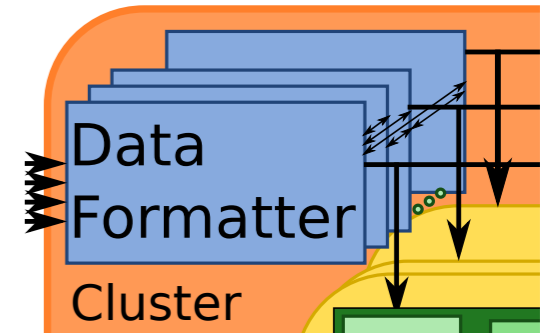
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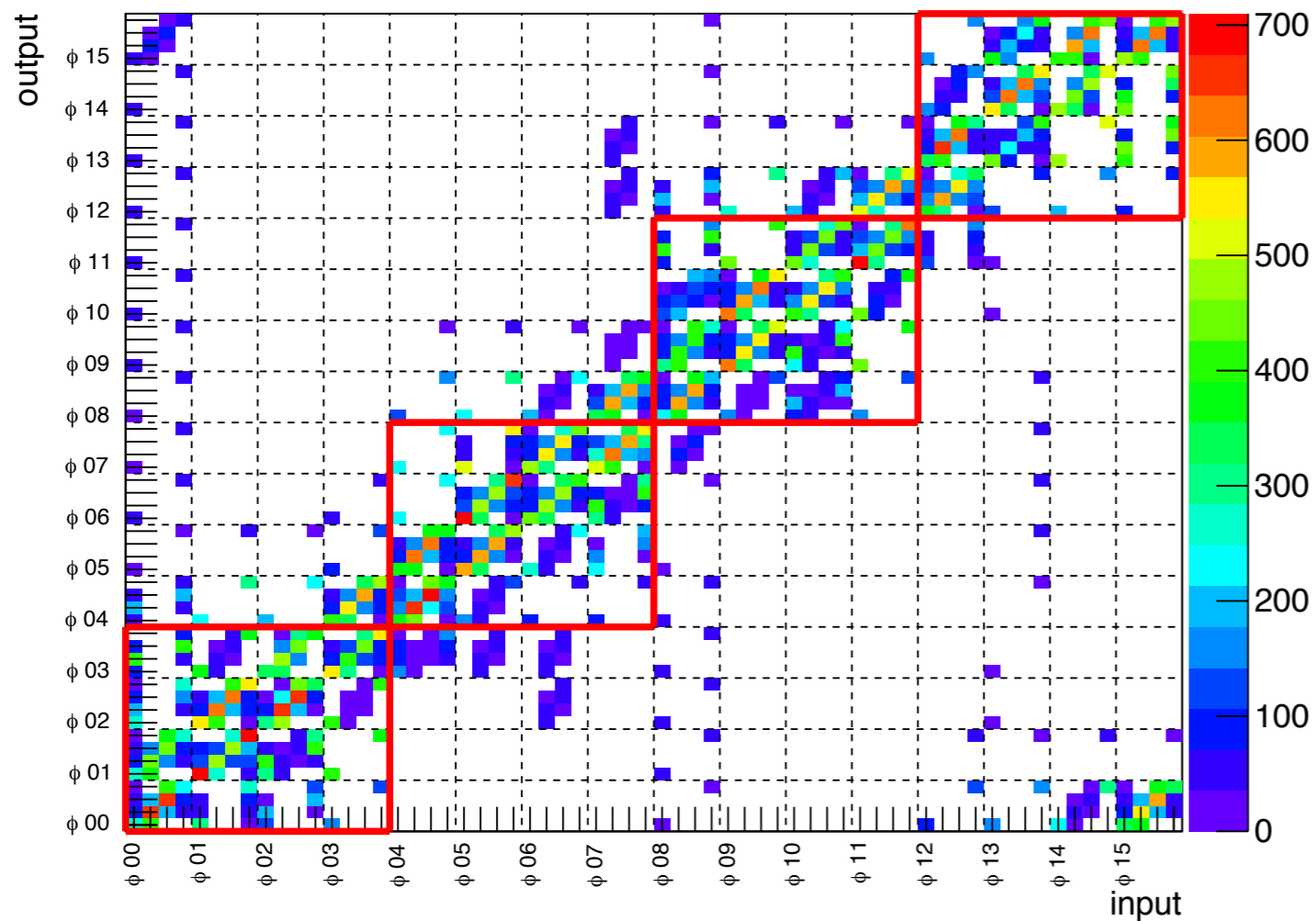
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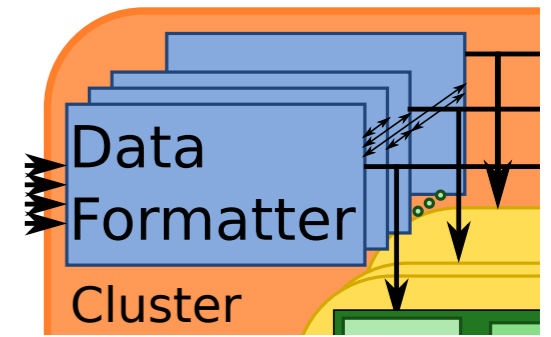
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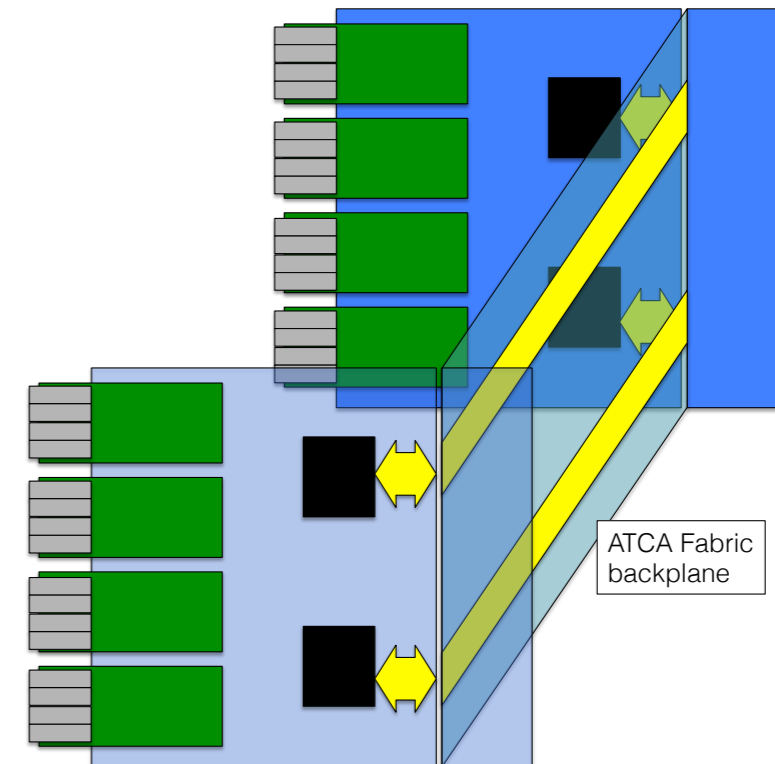
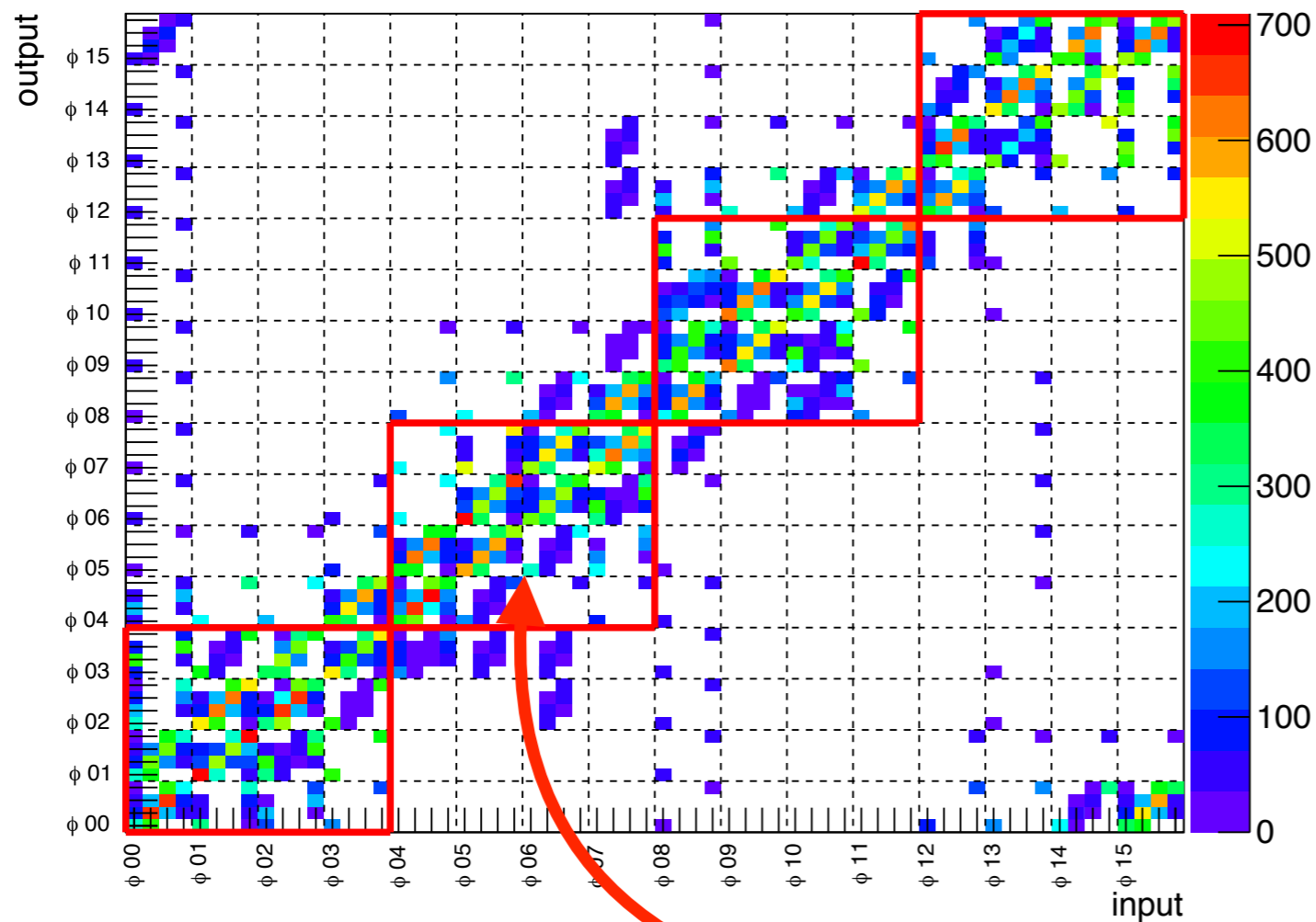
- Implemented in ATCA crates with full mesh backplane
- 32 DF boards in 4 crates
- Each DF connects to 2 towers



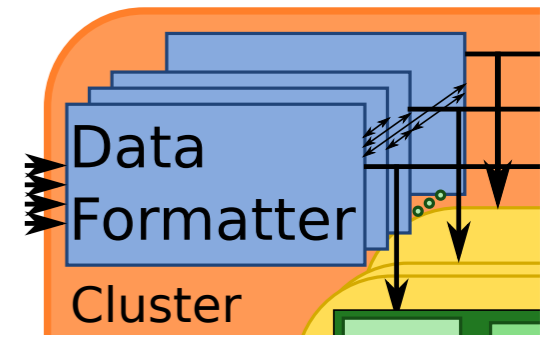
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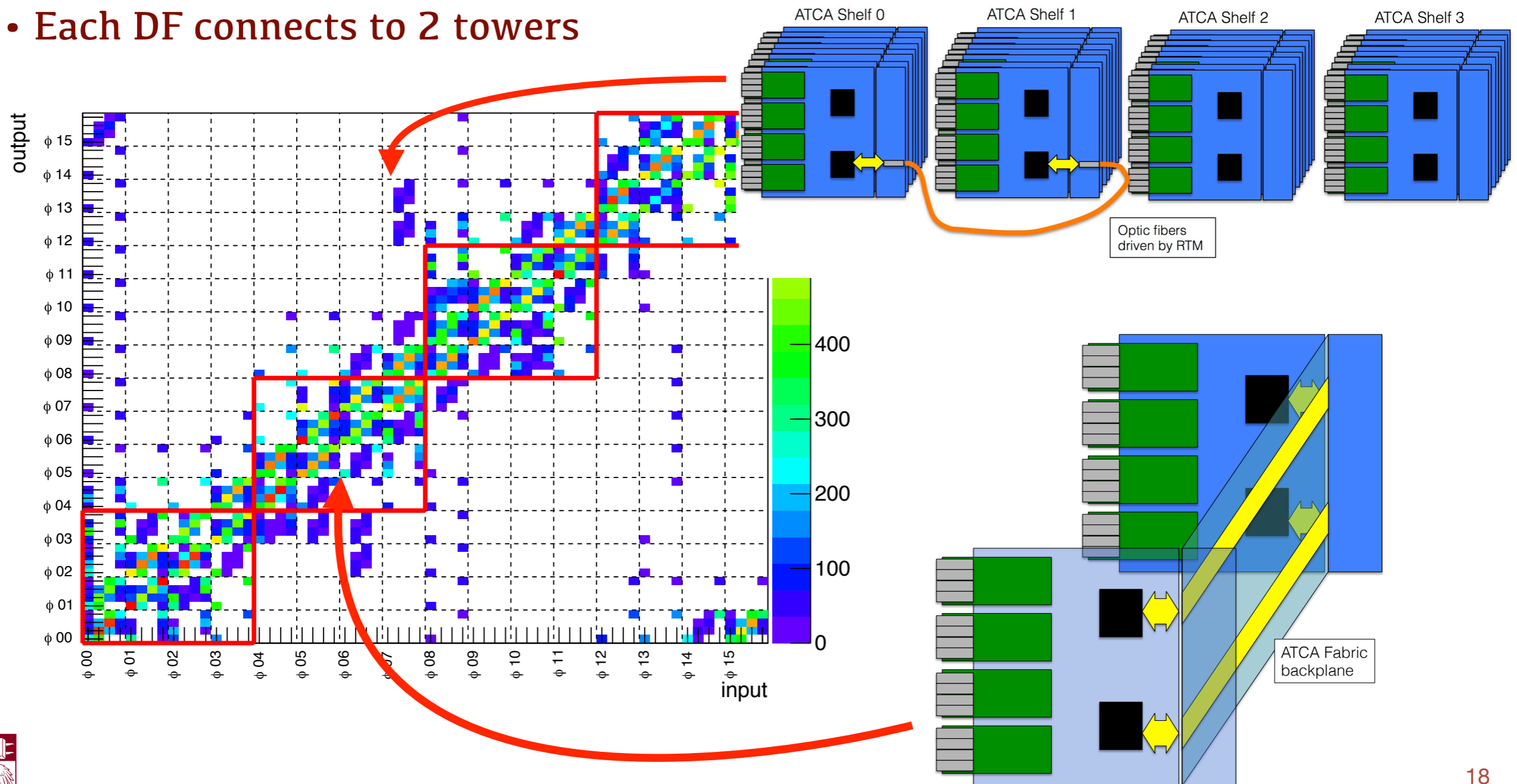
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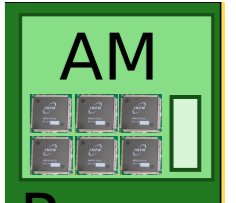


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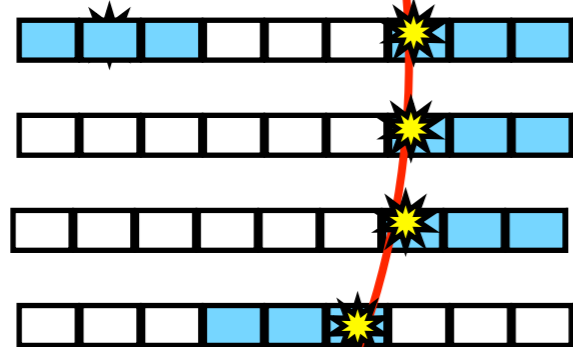


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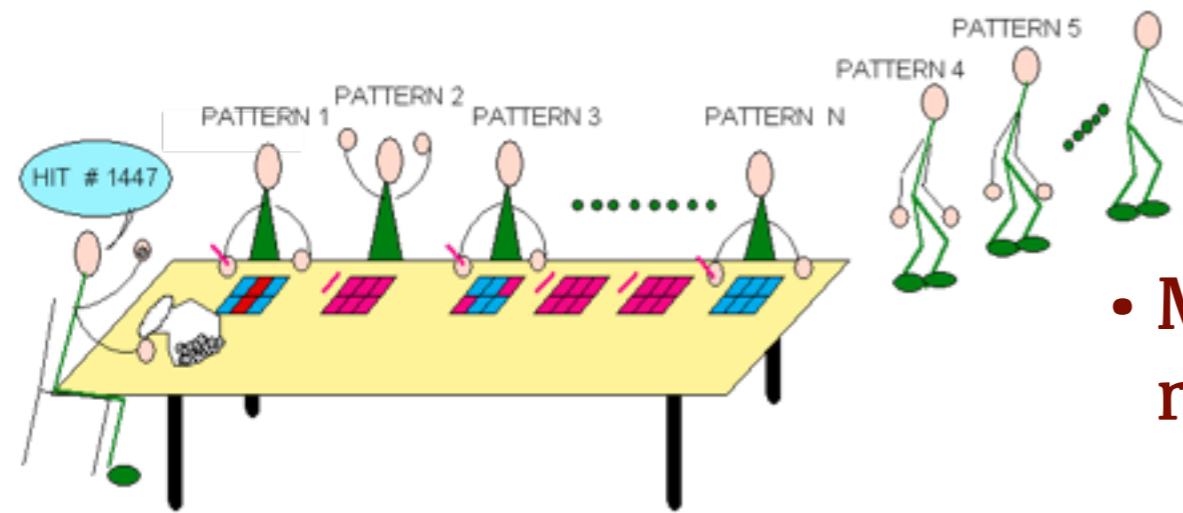




Stage 2: Pattern Recognition



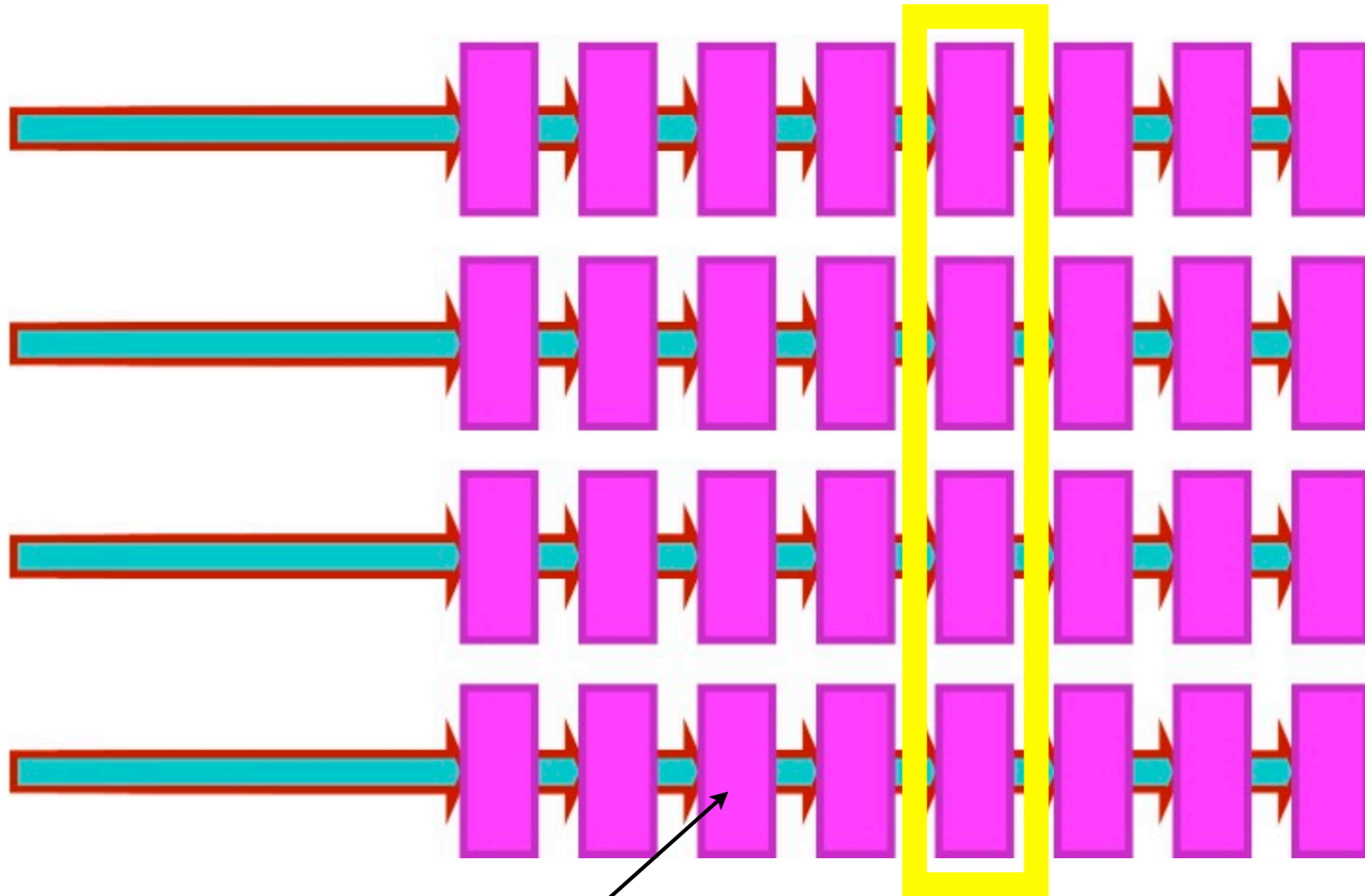
- Hits are ganged into Super Strips (SS)
 - Roughly 15x36 pixels/16strips per SS @ 70 int/x-ing
- **Custom associative memory chips** are used to compare hits to $O(10^9)$ patterns **simultaneously**
- Pattern matching finished as soon as all hits are read
- Matched patterns (Roads) are then fit to reject bad roads
 - Most matches are fake, need fits to reduce bad rate



Pattern Recognition Associative Memory

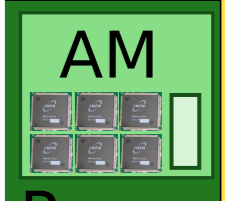
SS Busses by layer

Patterns



SSID

Pattern Recognition Associative Memory



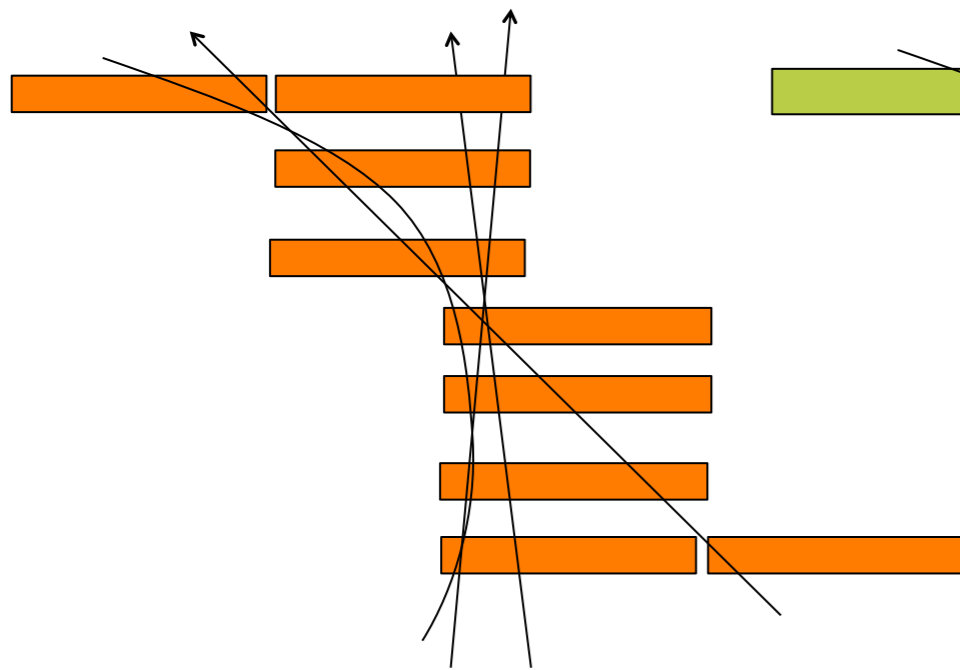
- Allows hits arriving at different times (but same event) to be compared!



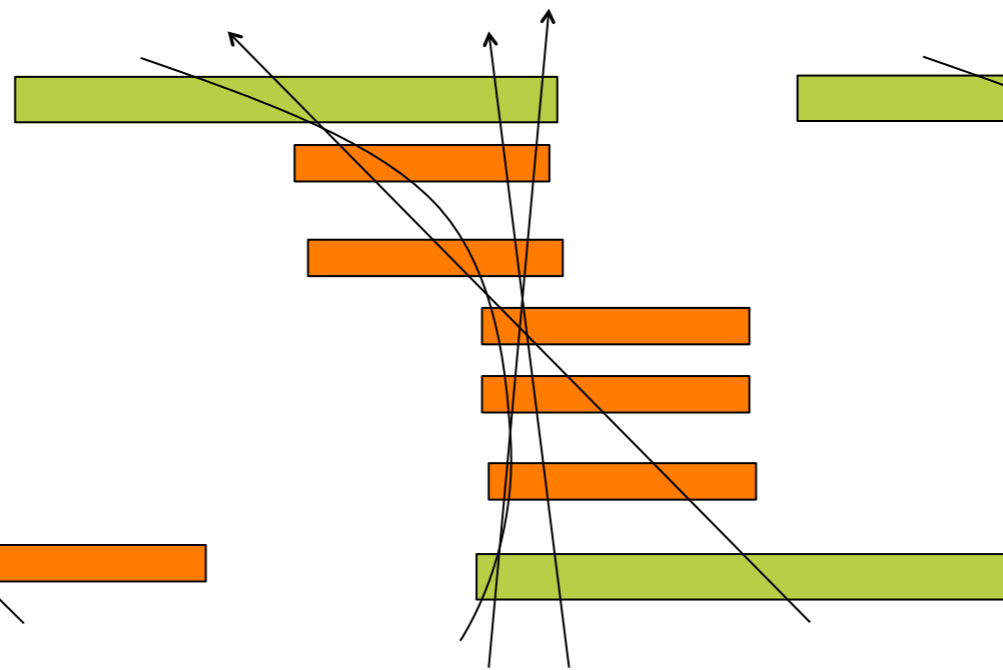
Refinements

- Majority Logic: Only require N out of M layers have a match
 - Gains efficiency
- Variable Resolution Patterns (Don't Care Bits)
 - Reduces the number of patterns and fake matches

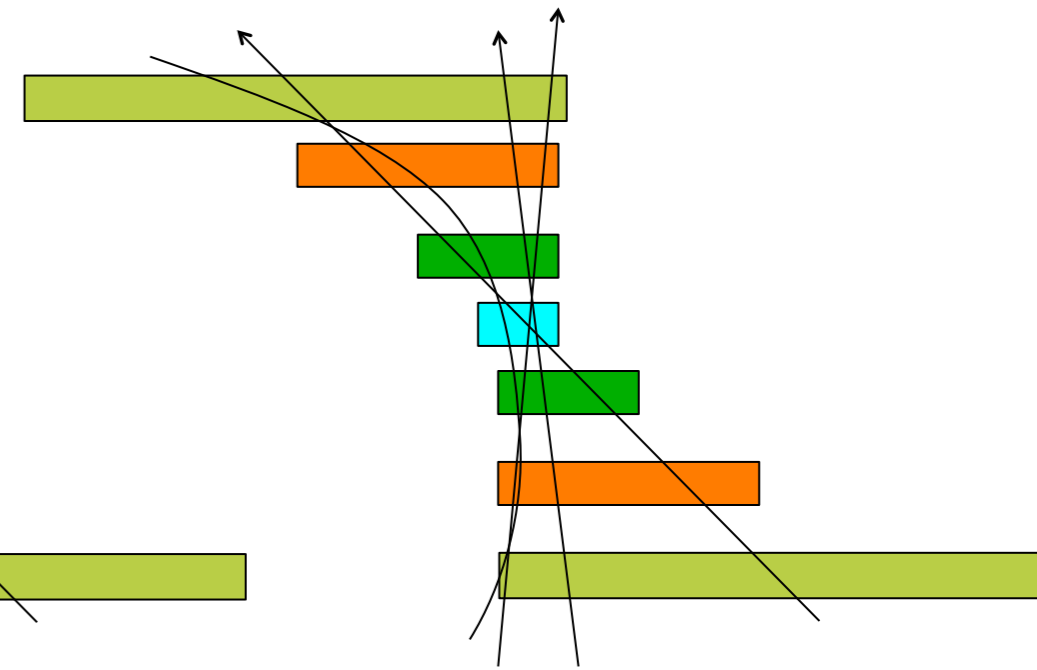
No variable resolution:
3 patterns needed



1 bit variable resolution:
1 pattern needed



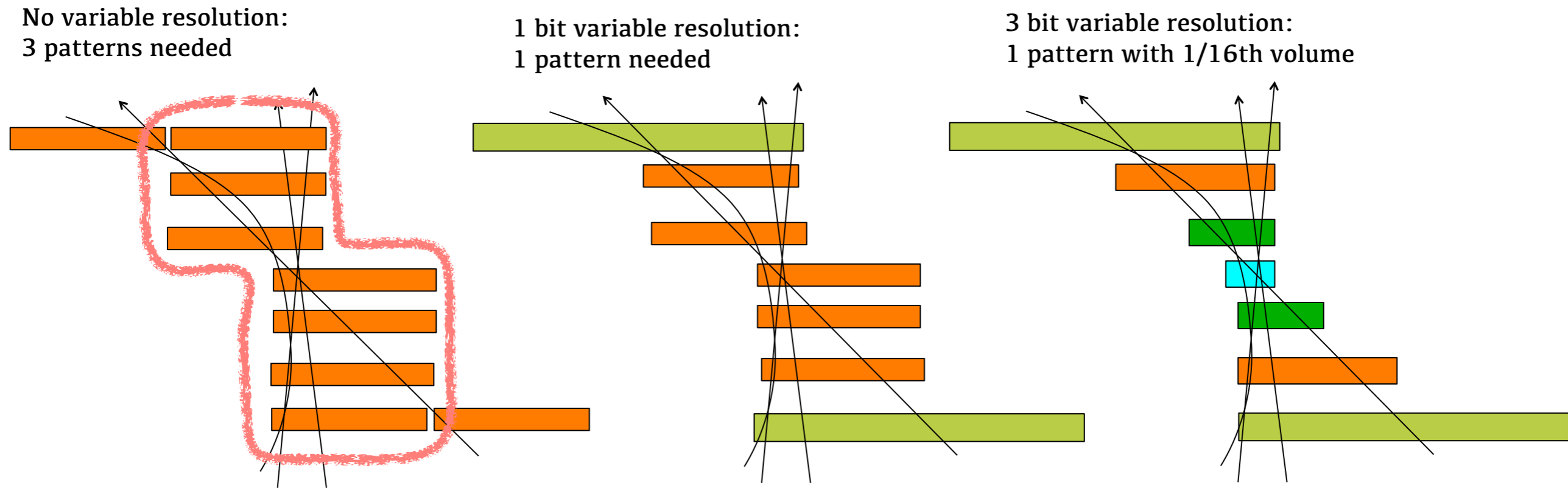
3 bit variable resolution:
1 pattern with 1/16th volume



- Number of don't care bits set on a layer by layer, pattern by pattern basis

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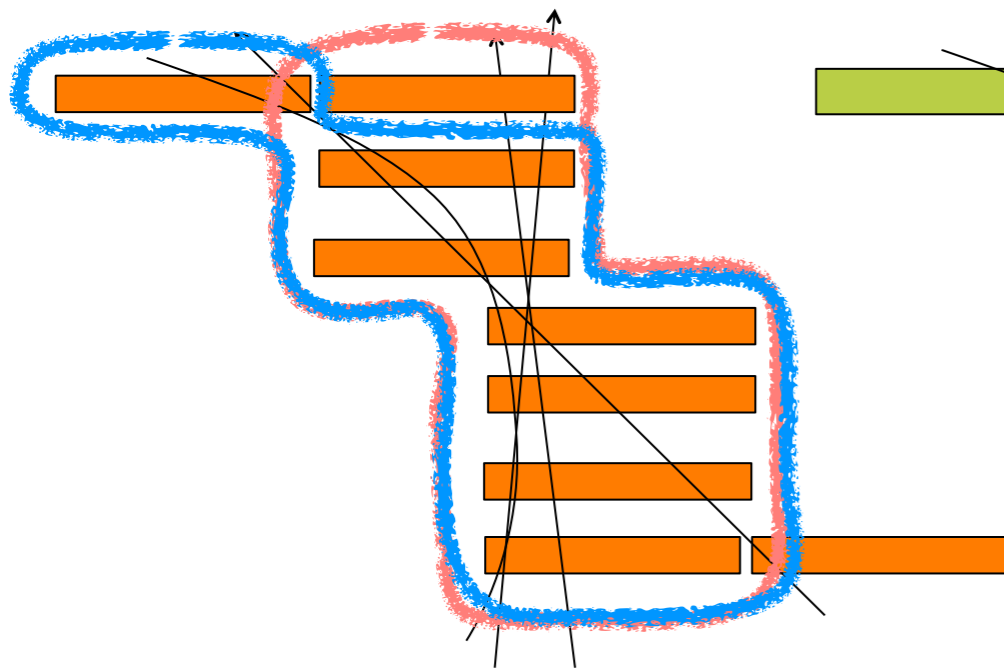


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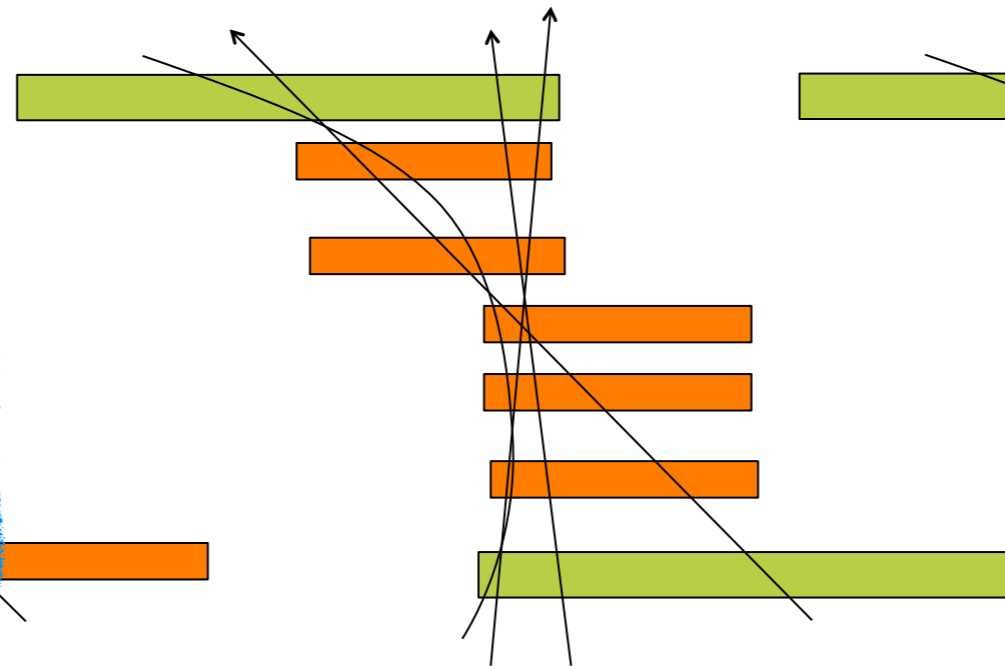
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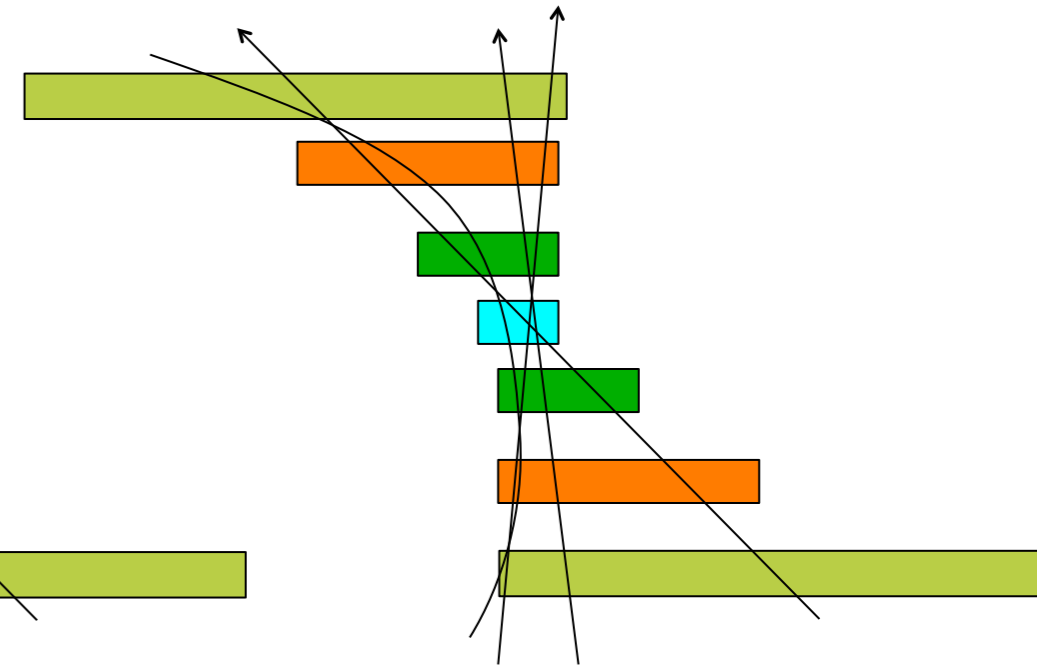
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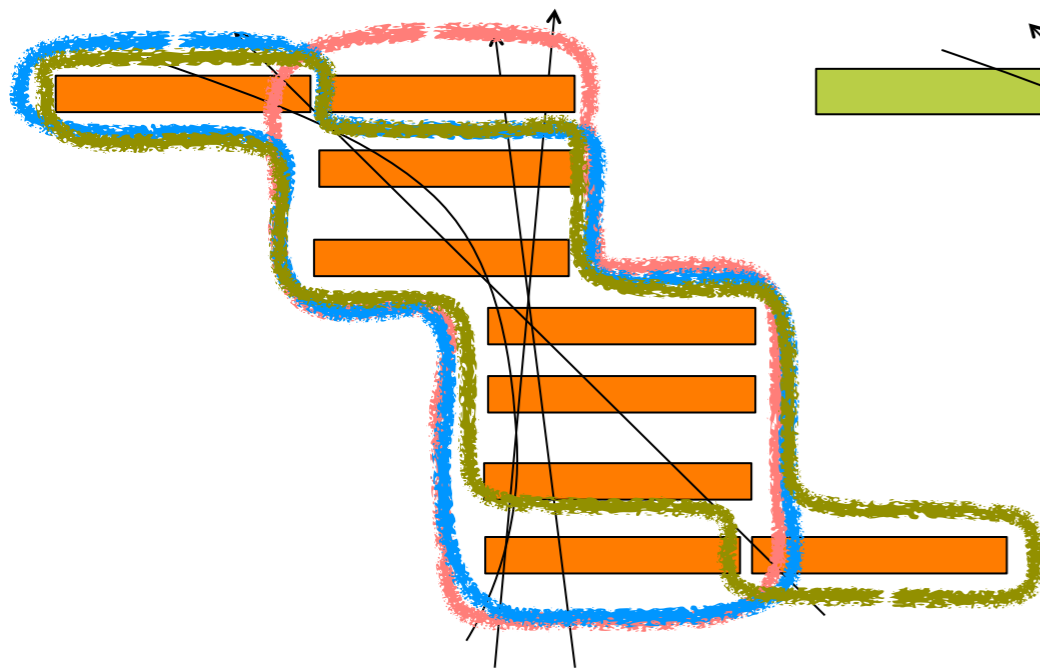


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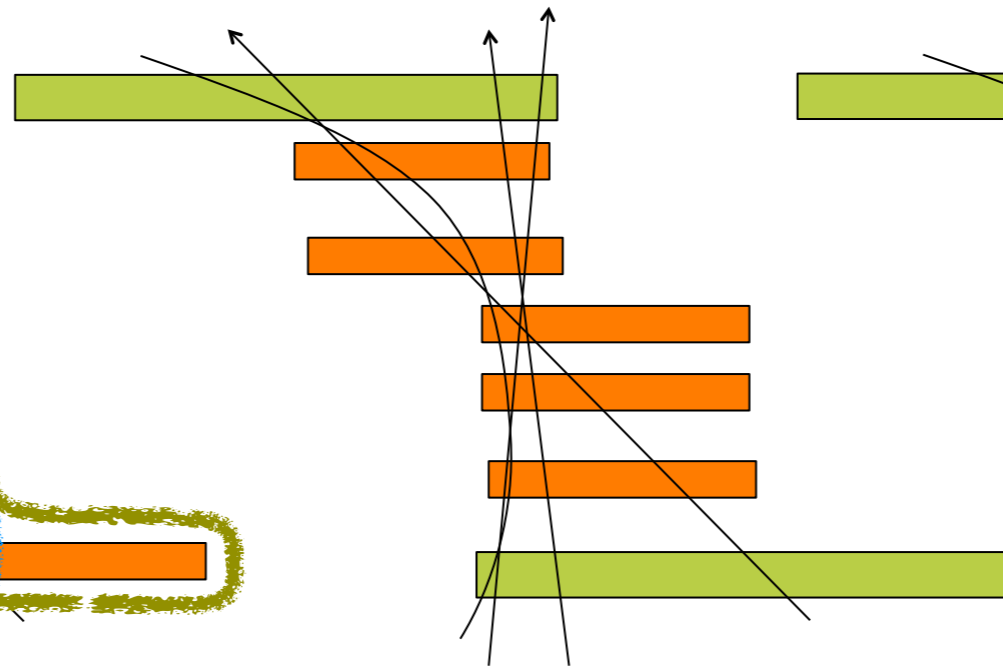
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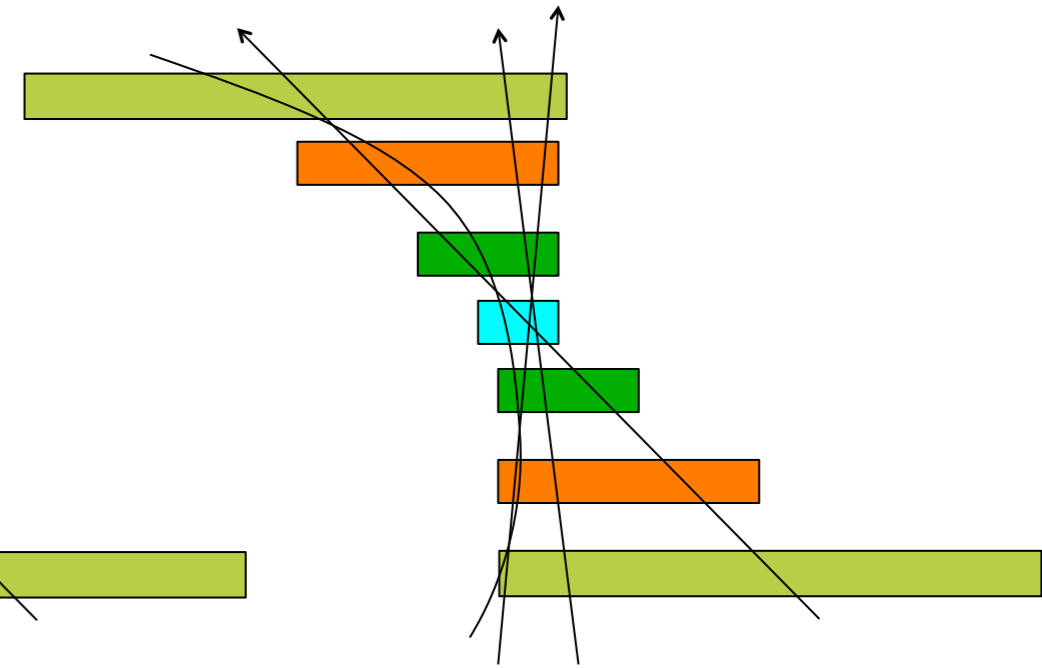
No variable resolution:
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1 bit variable resolution:
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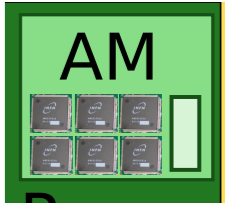


3 bit variable resolution:
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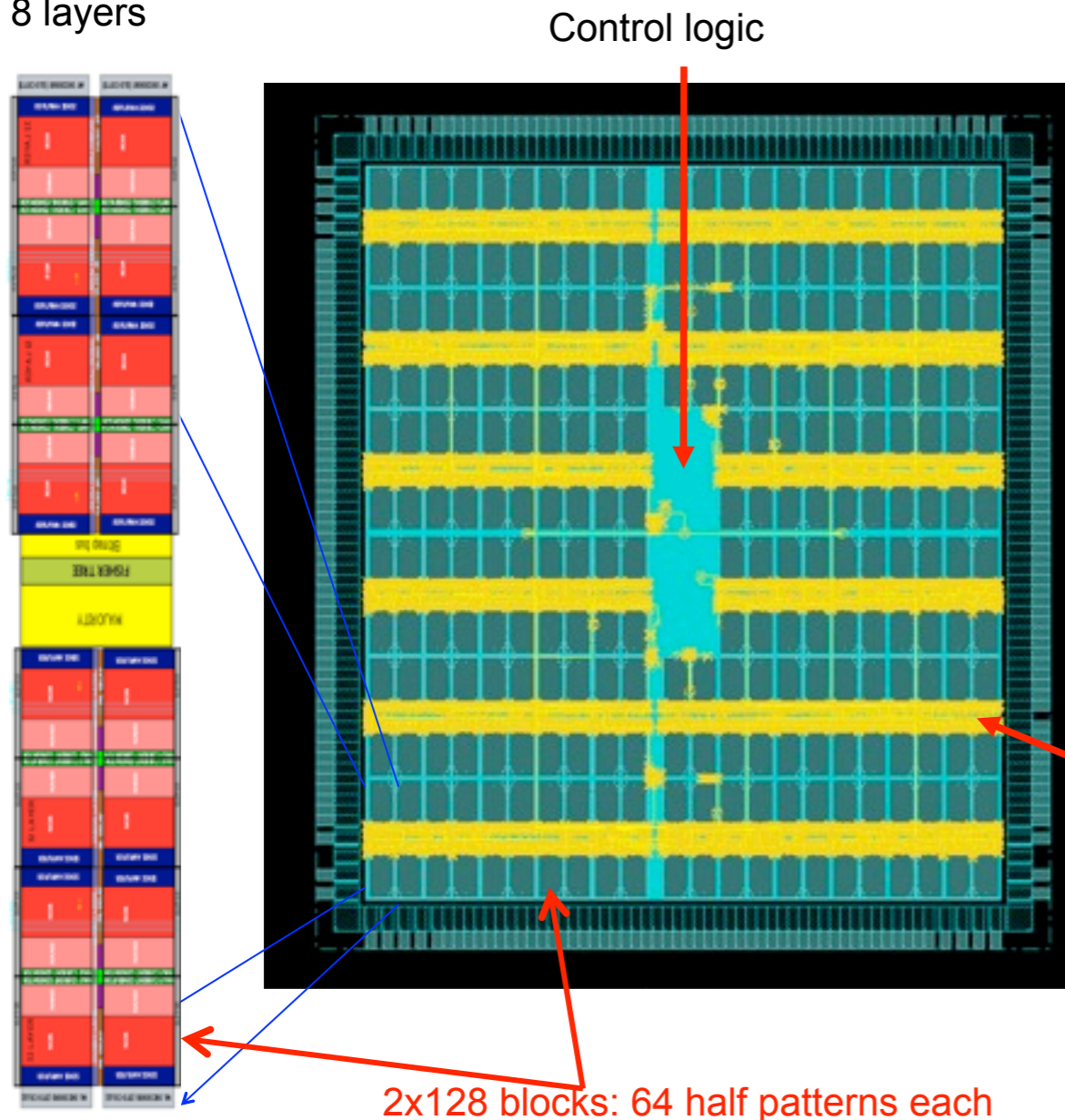


- Number of don't care bits set on a layer by layer, pattern by pattern basis

AMChips



64 patterns
x 8 layers



- **AM Chips: 64 nm custom associative memory chips**

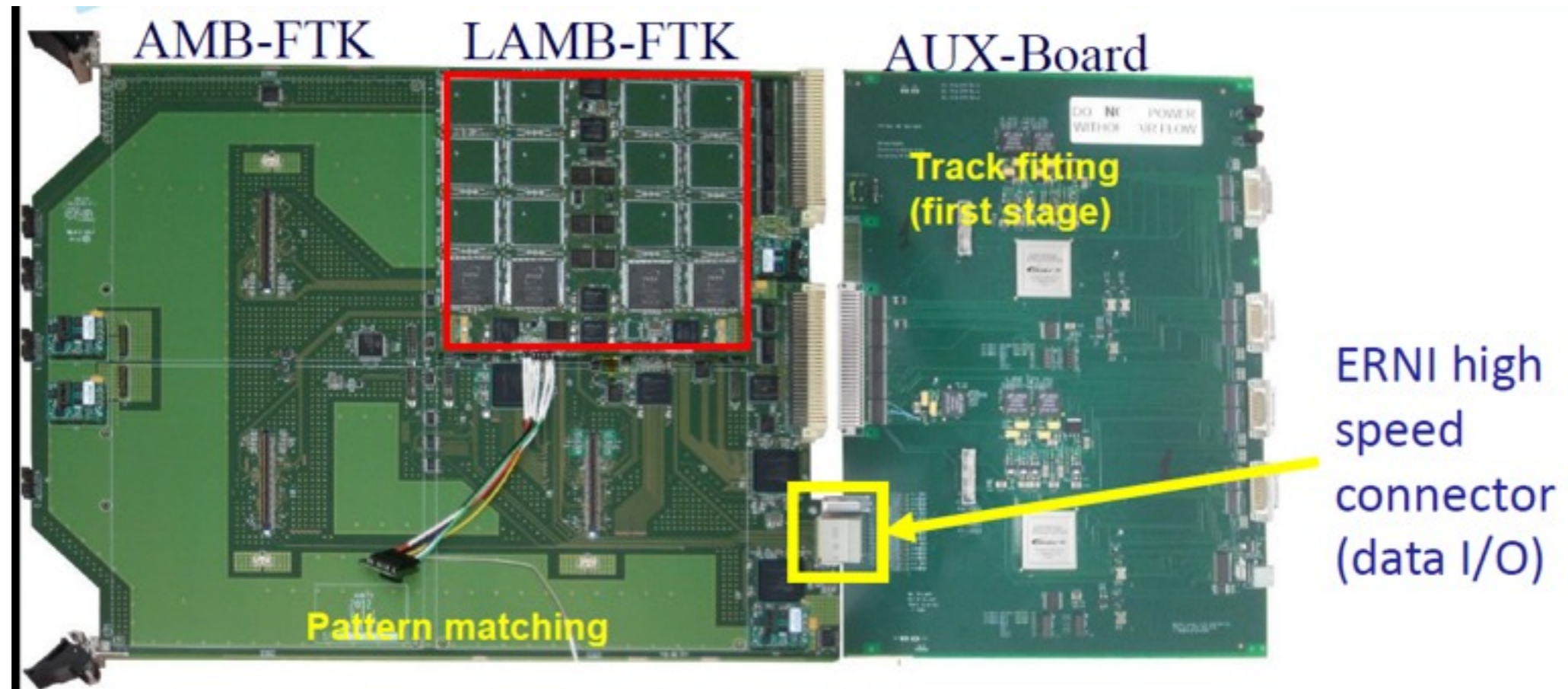
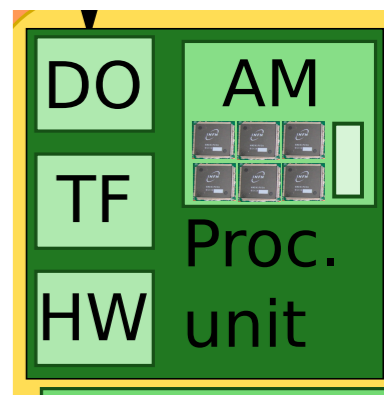
- 8 Layer (Pix + 4 axial SCT + 1 stereo SCT)
- 3-6 bits for variable resolution patterns
- Low power design: ~2W/chip, a factor 30-50 reduction in power/pattern/MHz over predecessor SVT chip

Majority logic and readout logic

- Functionality demonstrated in small area chips
 - 8k patterns



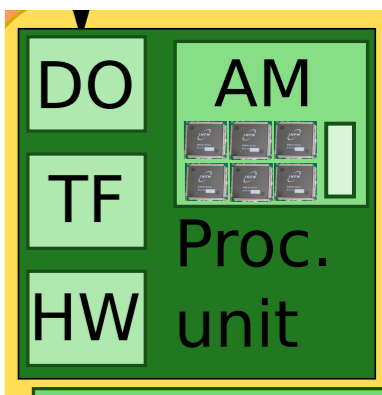
Processing Unit



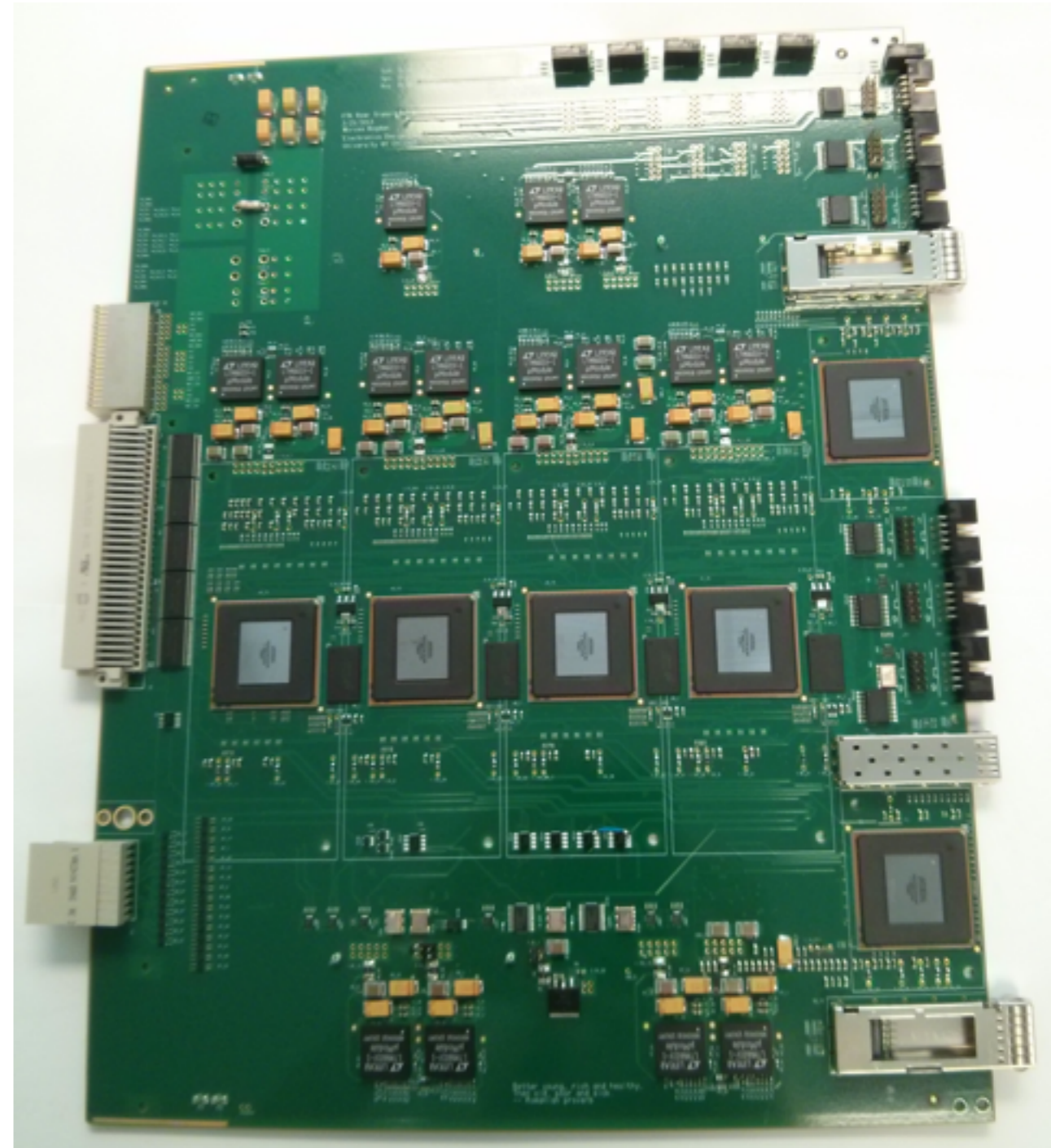
- AMChips found in Processing Unit:
 - AMboard + AUX Card
- Each AMBoard is composed of 4 LAMBs with AM chips
 - Each LAMB-FTK will contain 16 AMChips, $\sim 10^6$ patterns/LAMB
- AM Board + AUX communicate through P3 Connector
 - Successfully tested 2GBps transfer

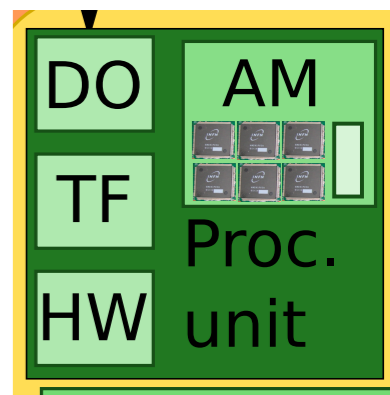


The AUX Card



- The AM Board has multifunctional Auxiliary Card
 - VME Control through main board through P2 connector
- Converts clusters to SS
- Receives matched road IDs and fetches full resolution hits
- Performs 8 layer fit to reject bad roads
- Sends roads to board for 12 layer fit

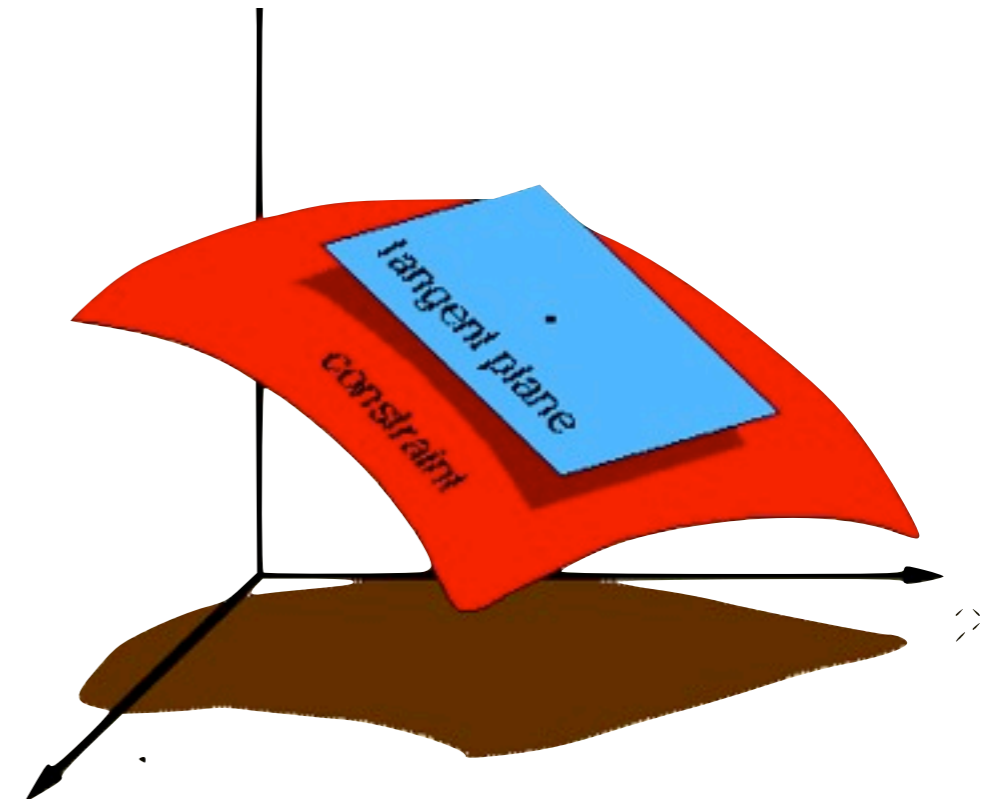
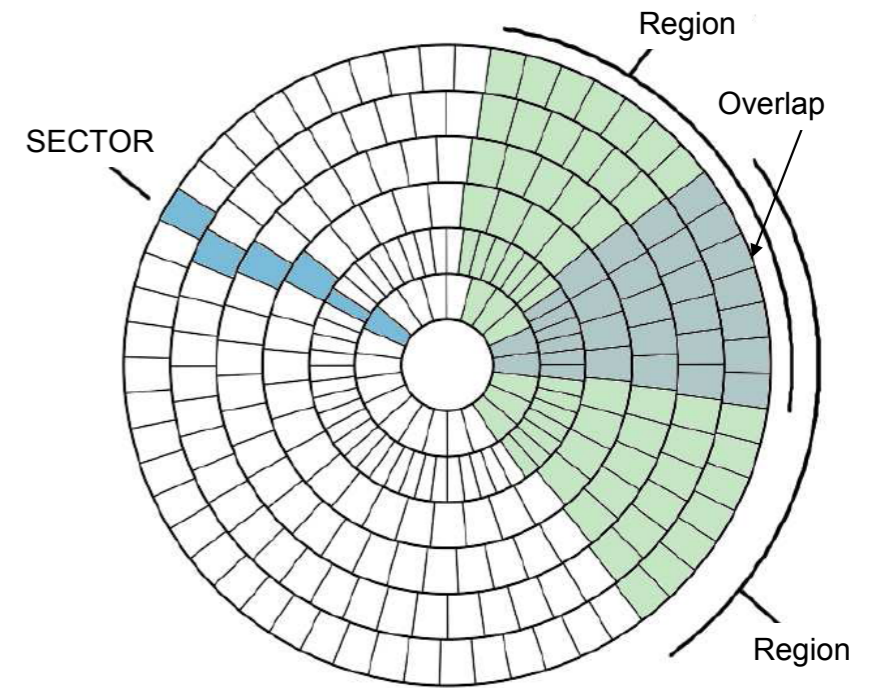




Linearized Track Fitting

- Fit constants predetermined and defined by sector
- FPGAs multiply and add coordinates by constants to get χ^2
- If a layer is missing, missing hit position is guessed so χ^2 can be calculated
- Keep roads with at least 1 good track
- Fit 1 track / ns (1 track every 5 ps for full system)!

$$\chi_i = \sum_{j=1}^{N_c} S_{ij} x_j + h_i; i = 1, \dots, N_\chi$$

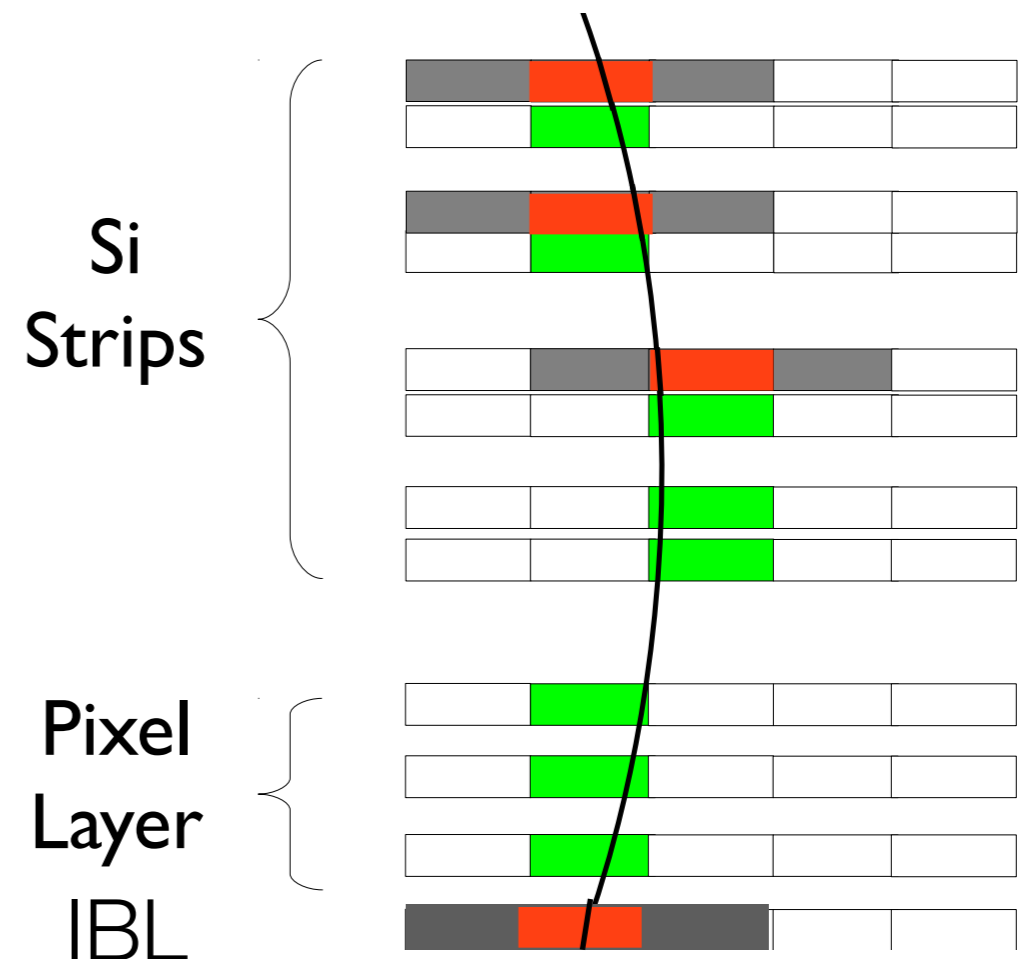


Stage 3: 12-layer Track Fitting

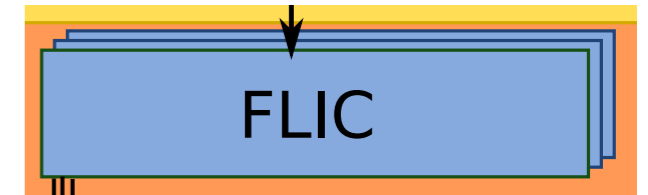
- Use constants precomputed from linearized constraints to guess hit coordinates

$$x'_i = \sum_{j=1}^{11} H_{ij} x_j + g_i; i = 1, \dots, N_\chi$$

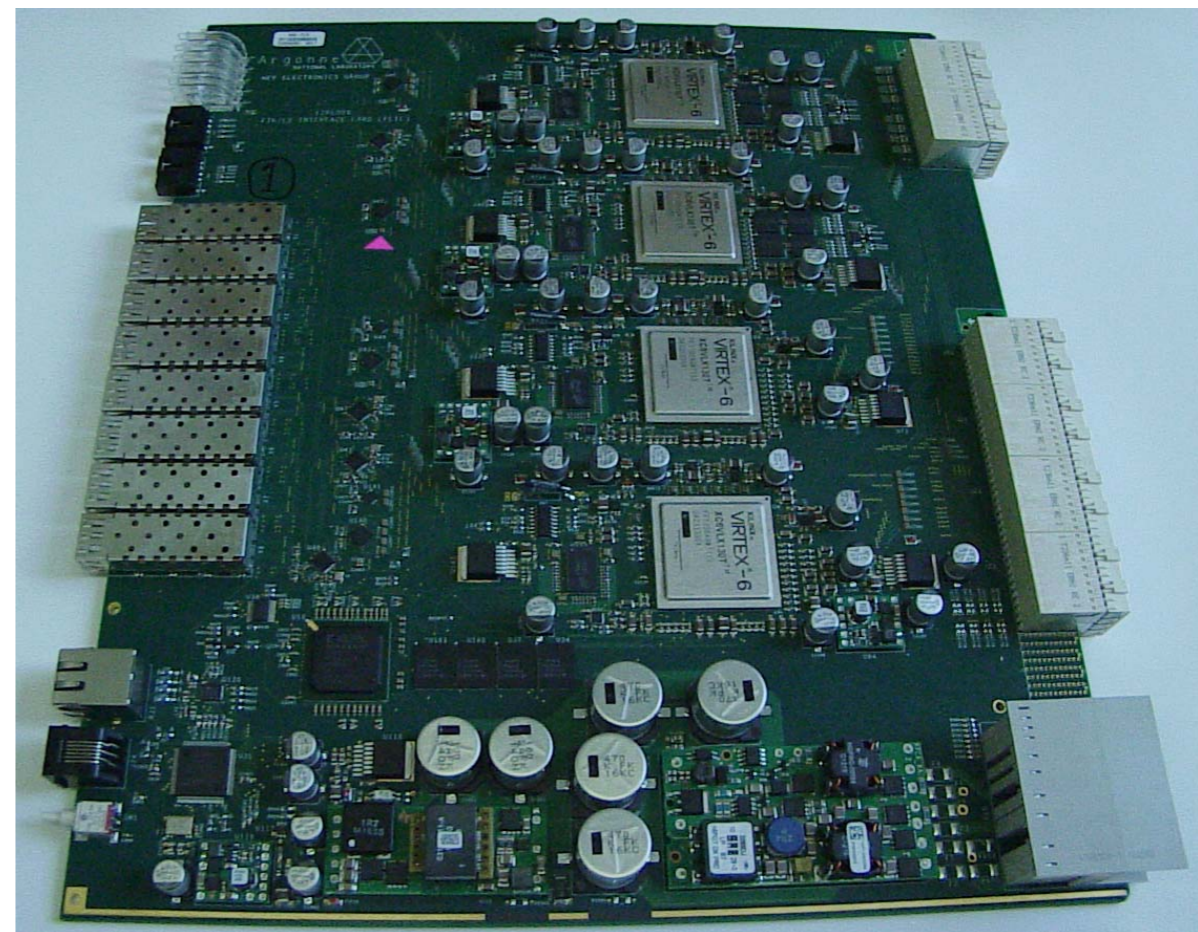
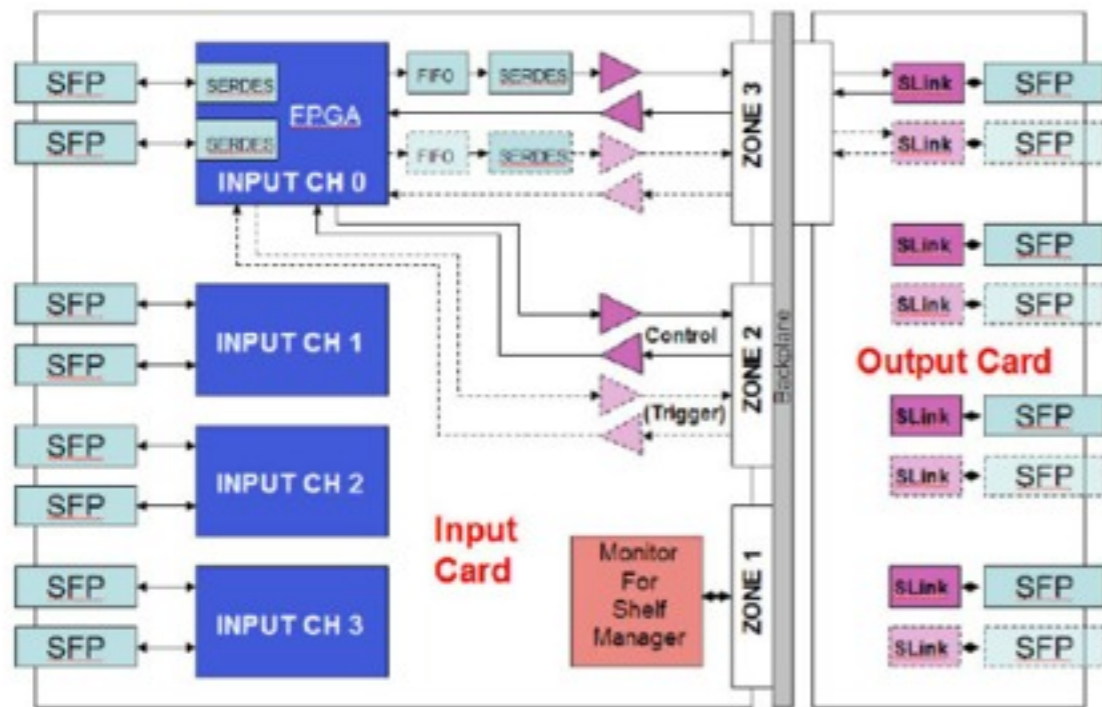
- Find matching SS
- Refit with good hits to find best χ^2 and track parameters
- Good tracks, with parameters, hits and errors are sent to final crate for formatting for L2



FTK to Level 2

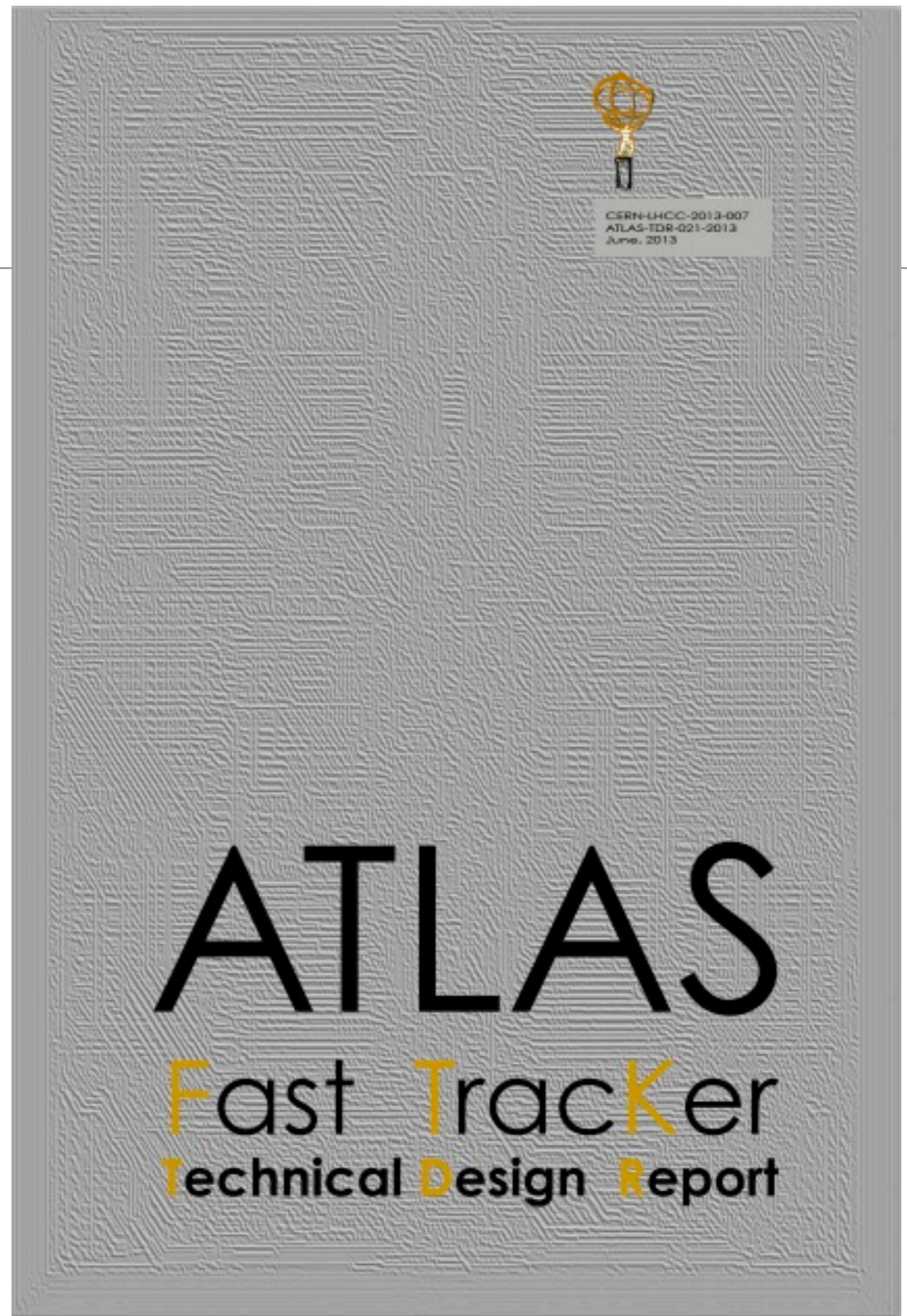


- FTK to Level 2 Interface Crate connects FTK to HLT
 - Formats data for HLT
 - Also does monitoring and control
- Uses dual-star ATCA crate
 - Will allow for local trigger processing (primary vertex finding, beamspot, MET, etc.) in the future



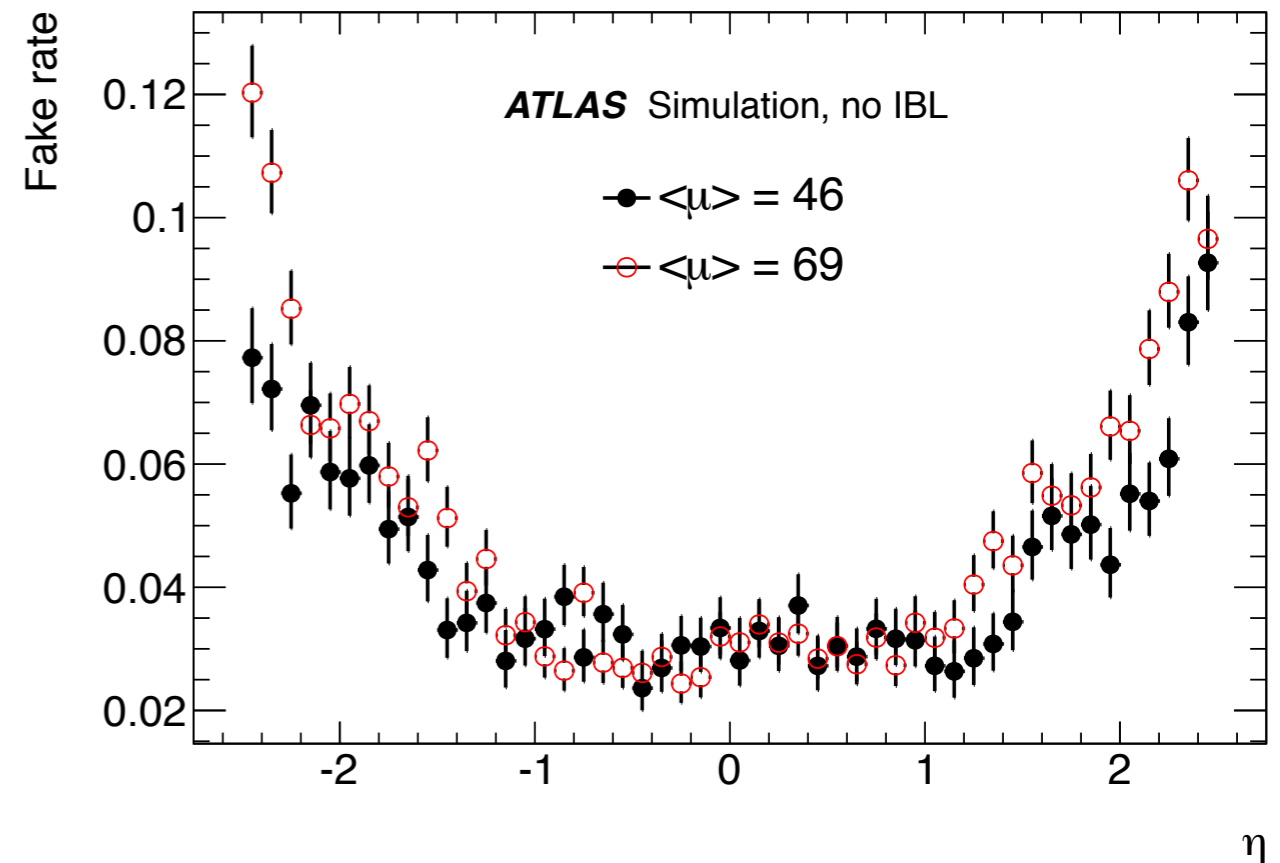
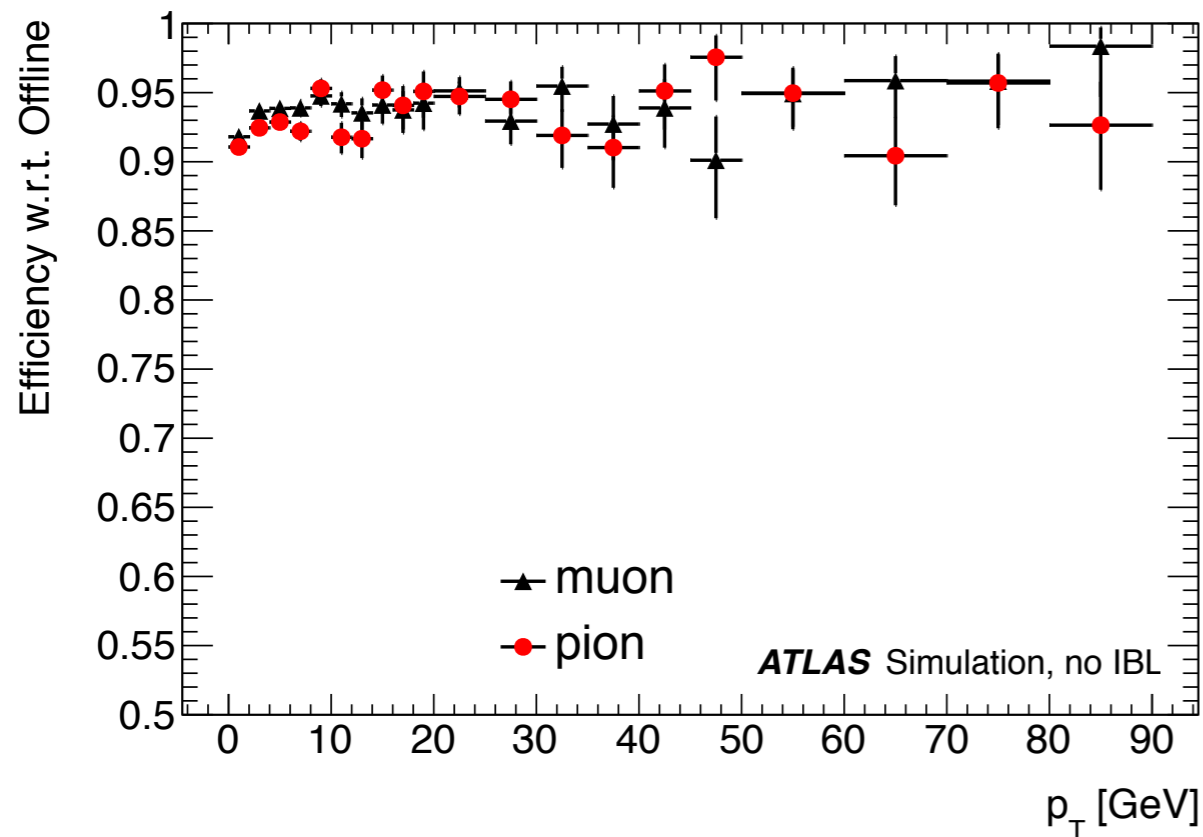
Performance

- FTK has a detailed simulation of system logic for design and performance studies
 - Bit-level emulation in progress
- Performance shown in Technical Design Report from May 2013
 - <https://cds.cern.ch/record/1552953/>
 - Uses only 11 silicon layer (no IBL)



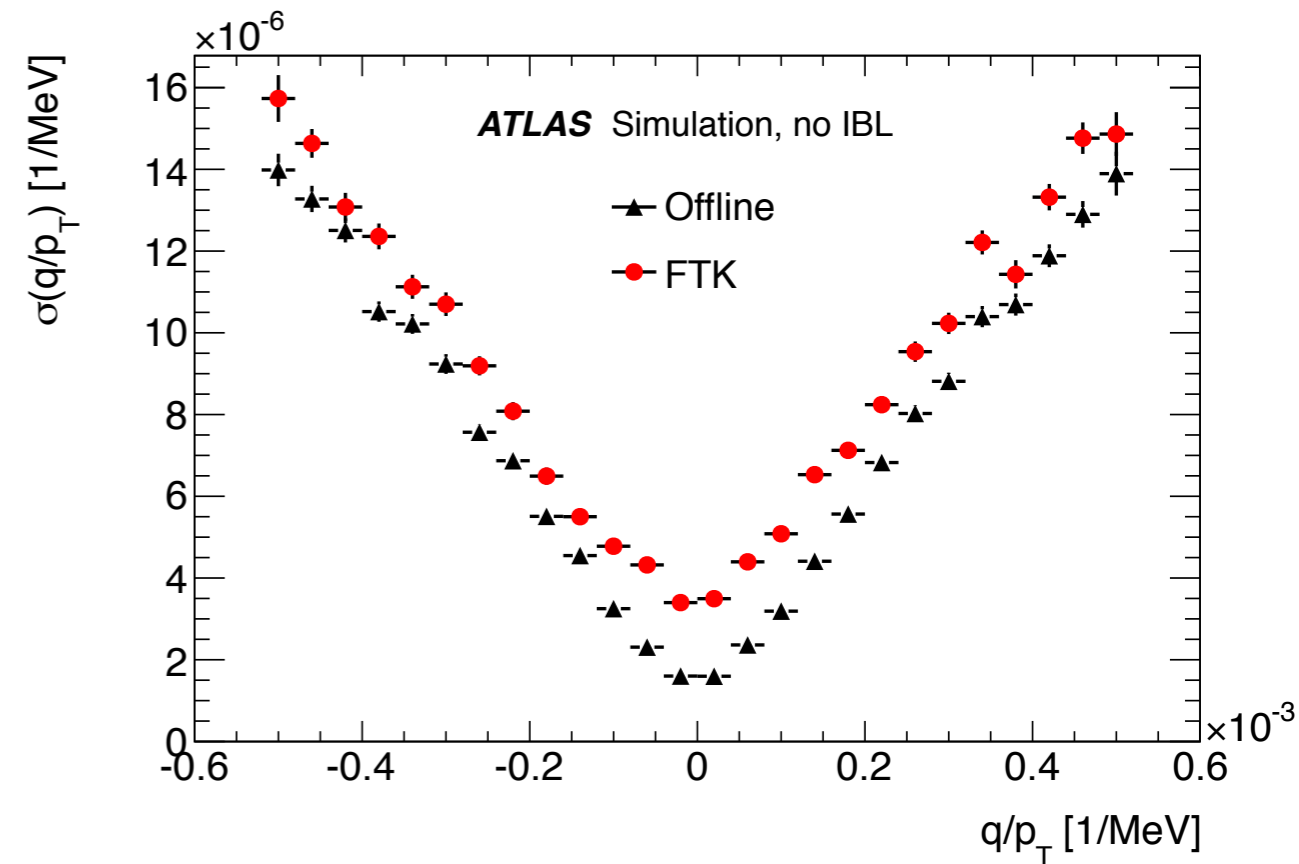
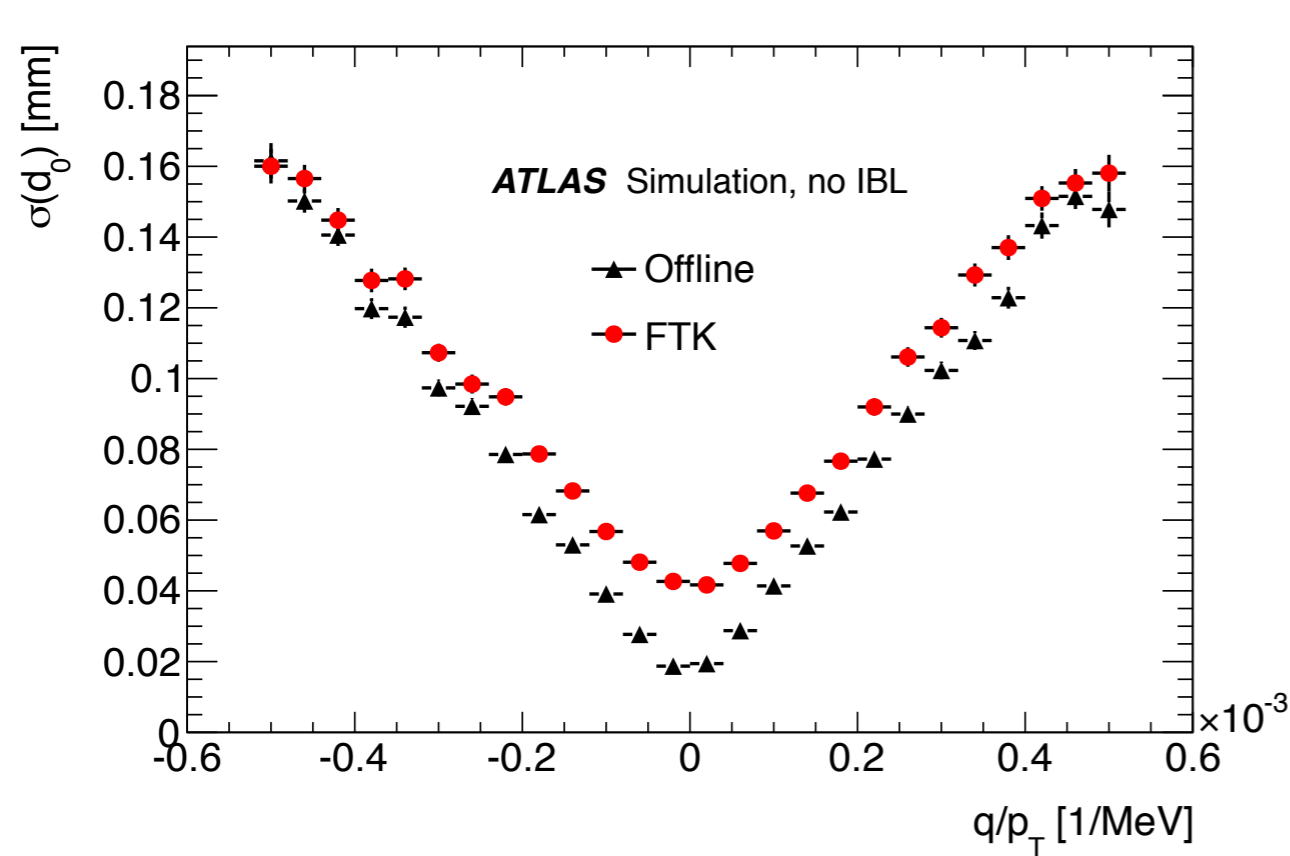
Efficiencies & Fake Rates

- 93-94% efficiency with respect to offline tracks
- 3% fake rate at central eta, up to 10% at high eta
- Actively working in improving efficiencies and fake rates



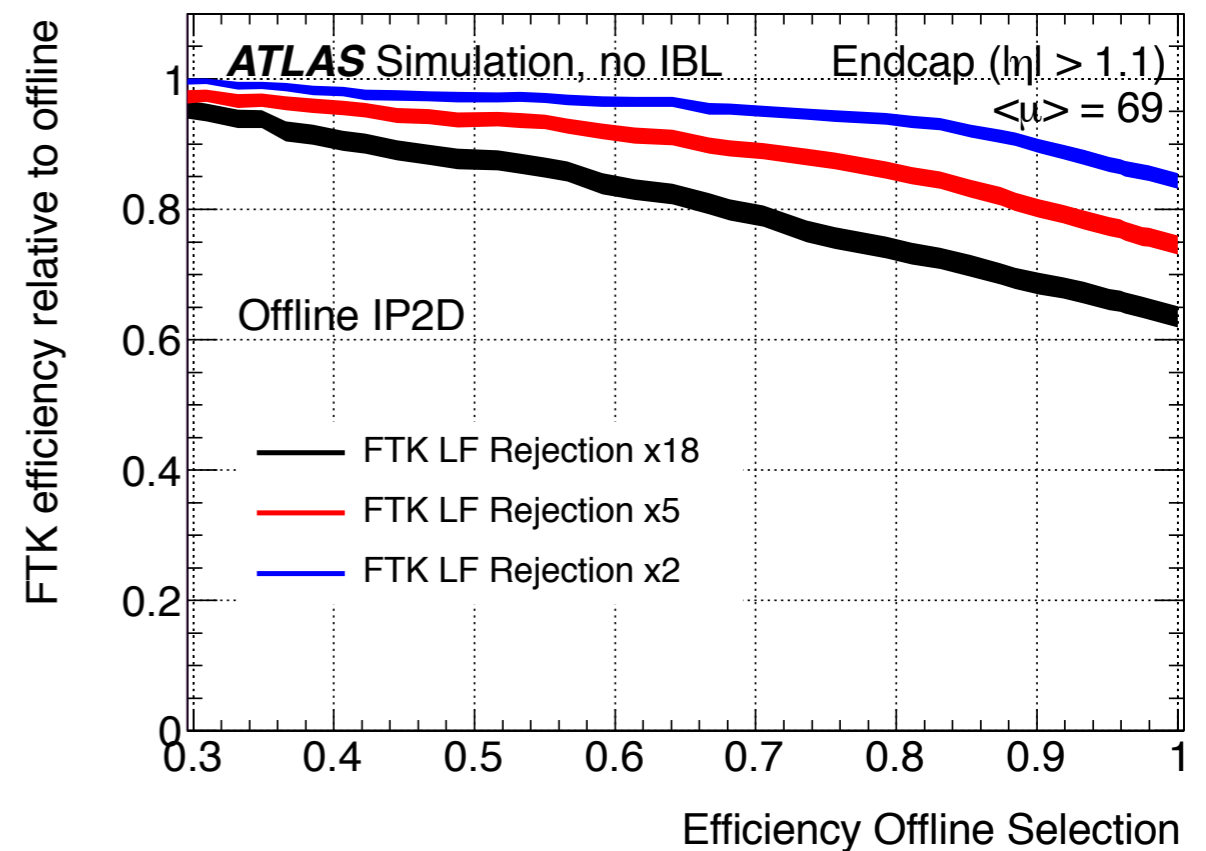
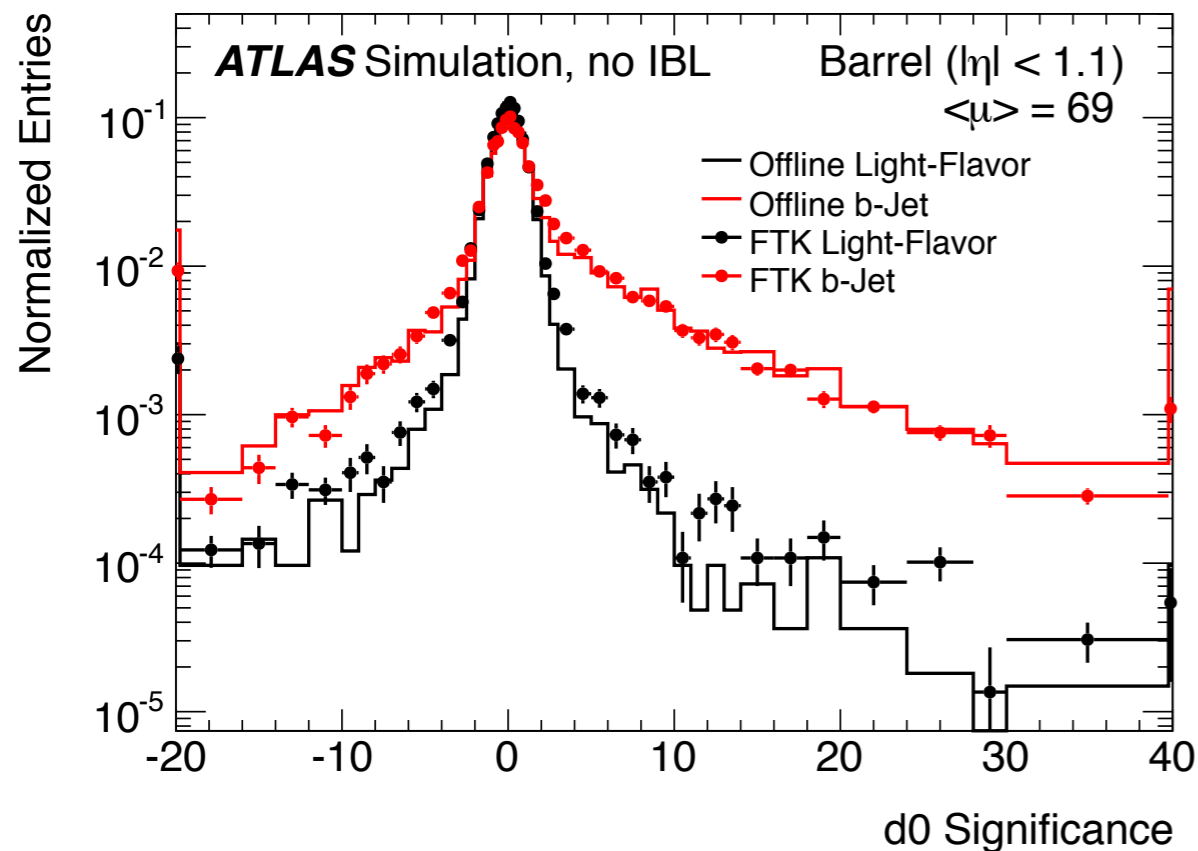
Performance: Resolutions

- Similar resolution to offline at low p_T , 2x worse at highest p_T
 - Improved with some clustering changes (not shown here)



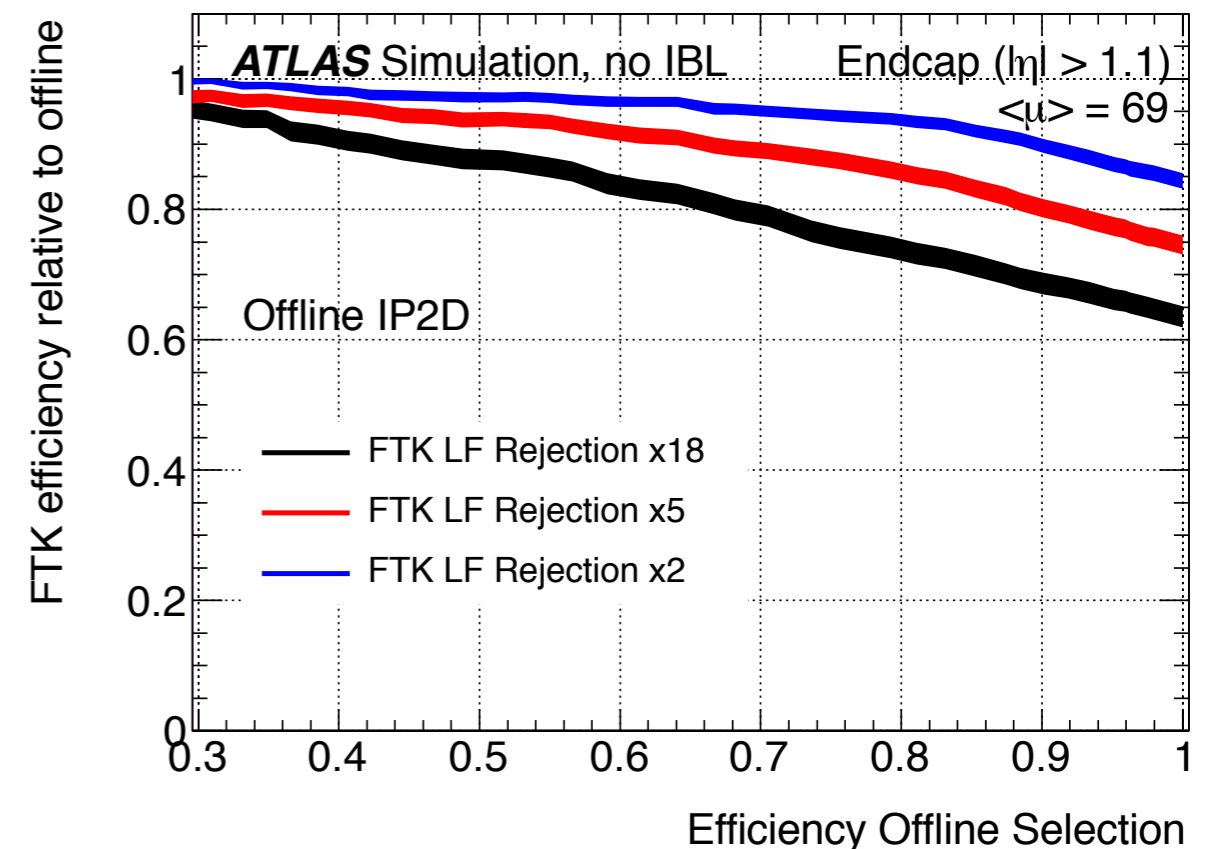
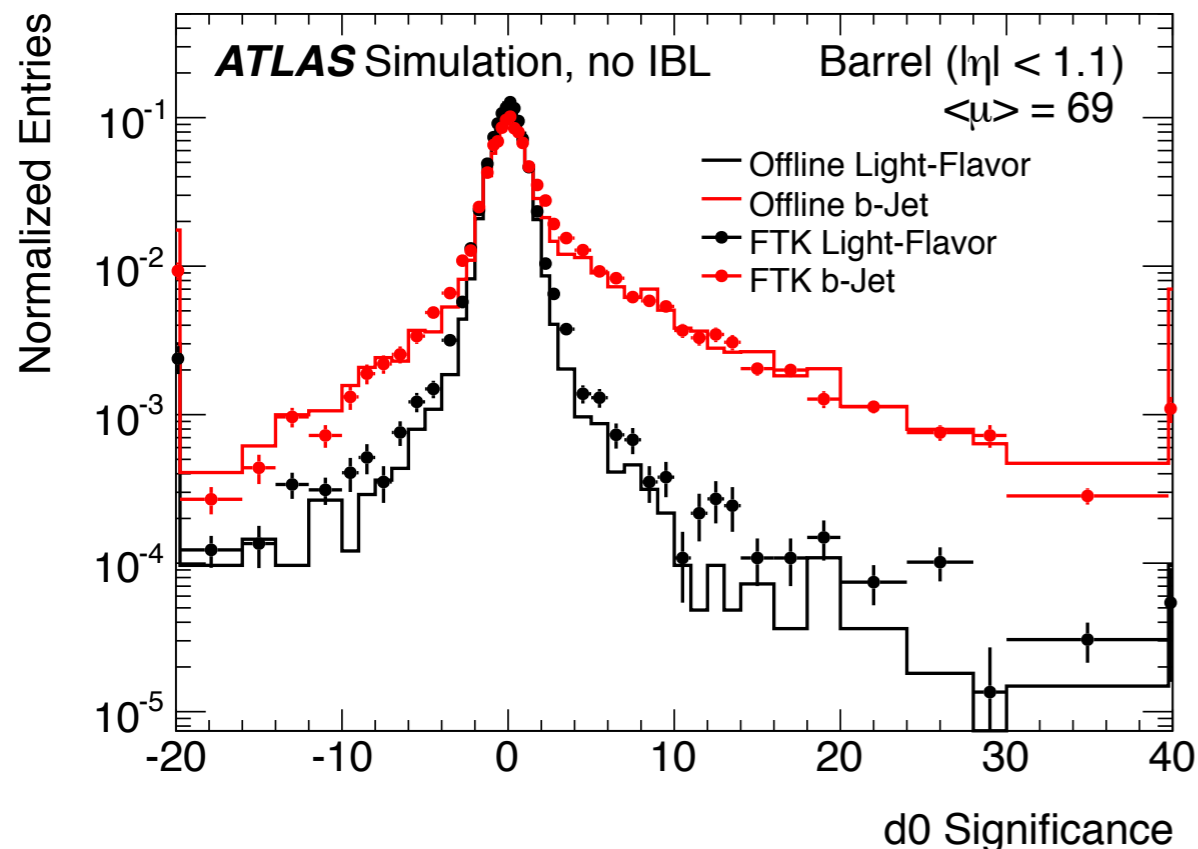
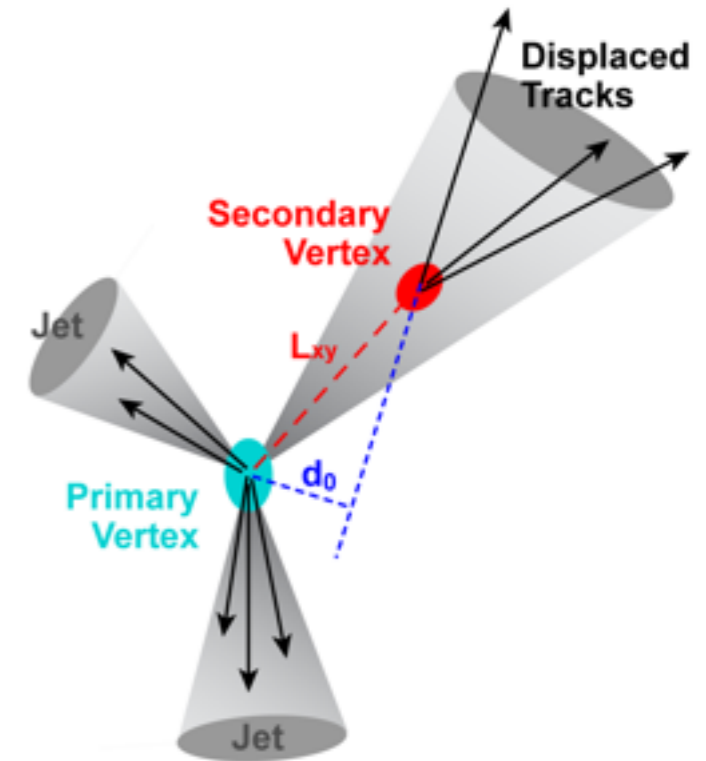
Performance: B-tagging

- Use simple 2D Impact parameter significance b-tagger
- For 80% offline point can get 70% or higher relative FTK efficiency
 - Even better relative performance when IBL is included



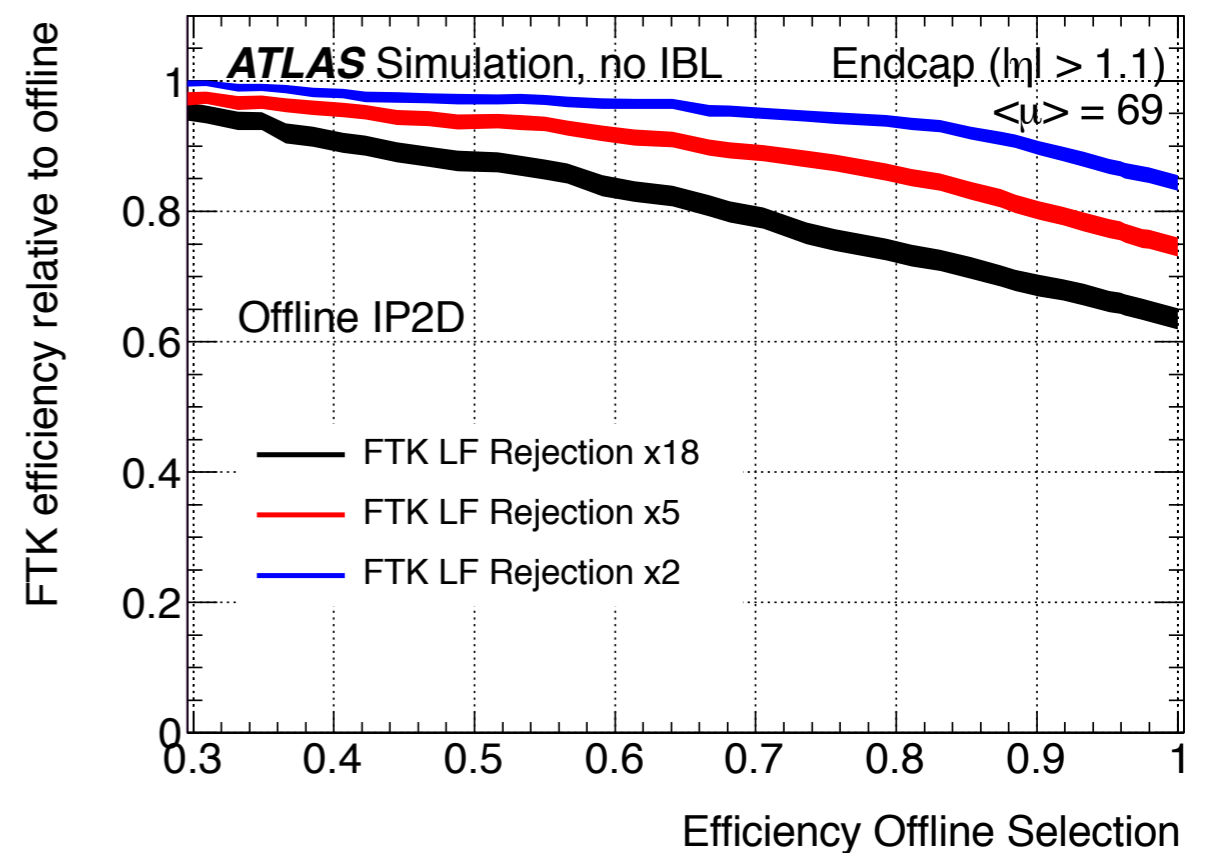
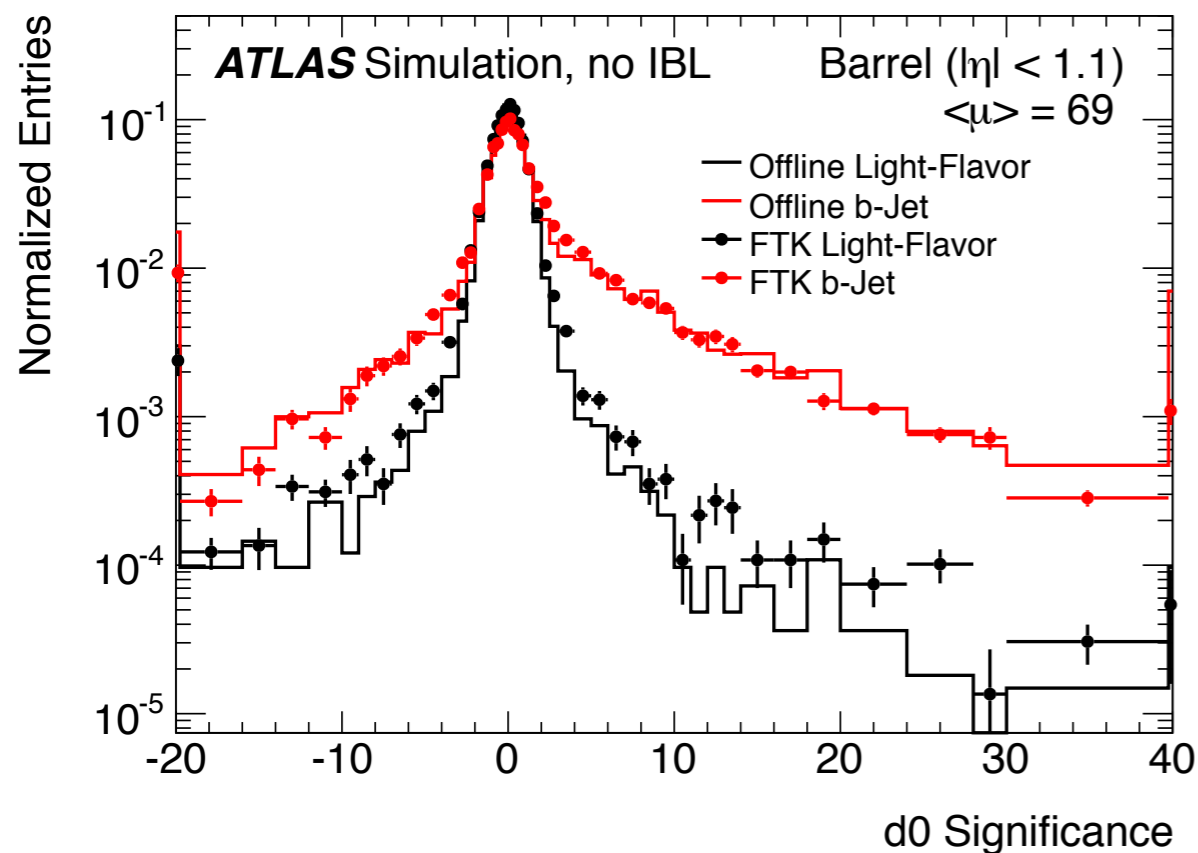
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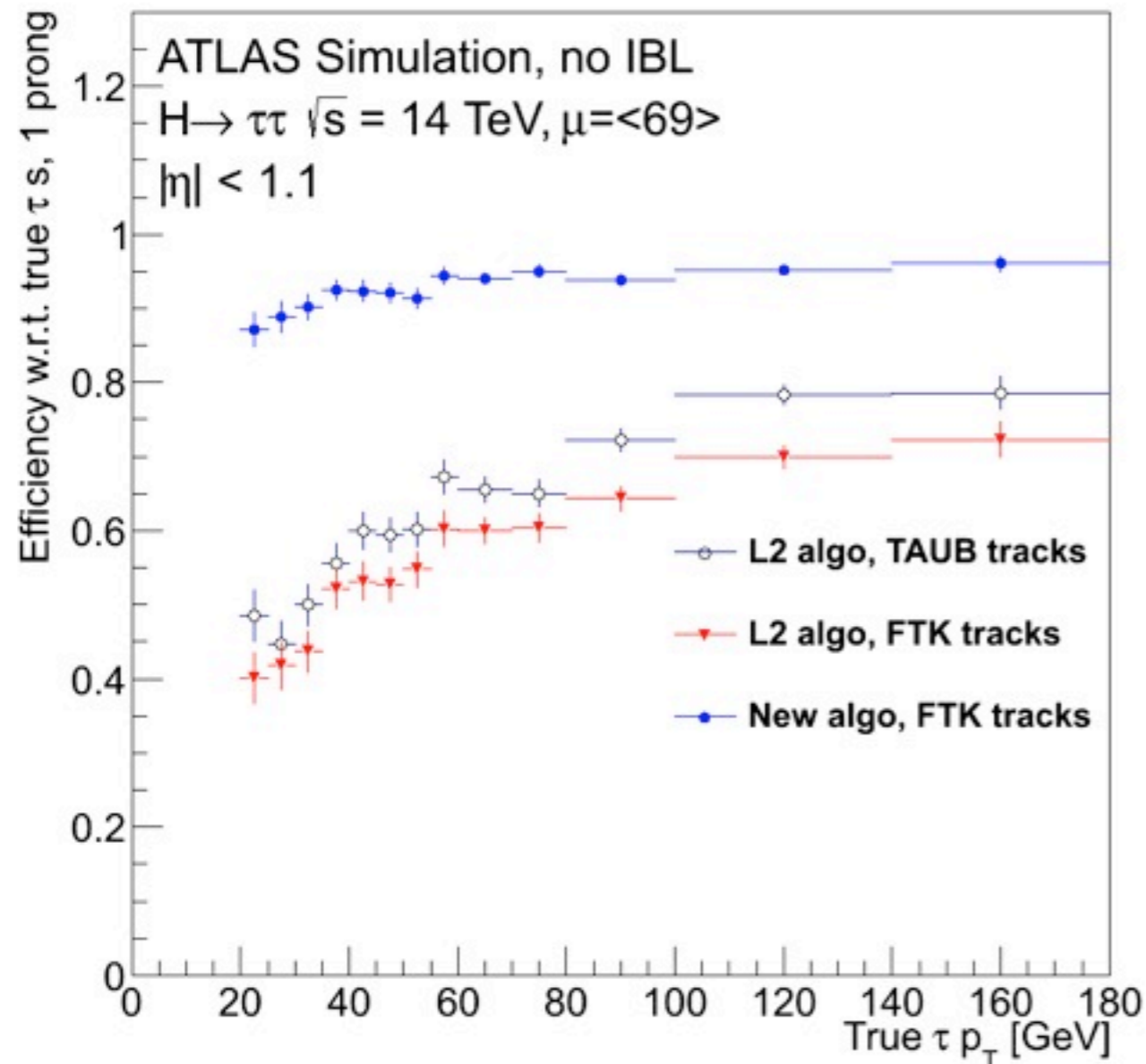


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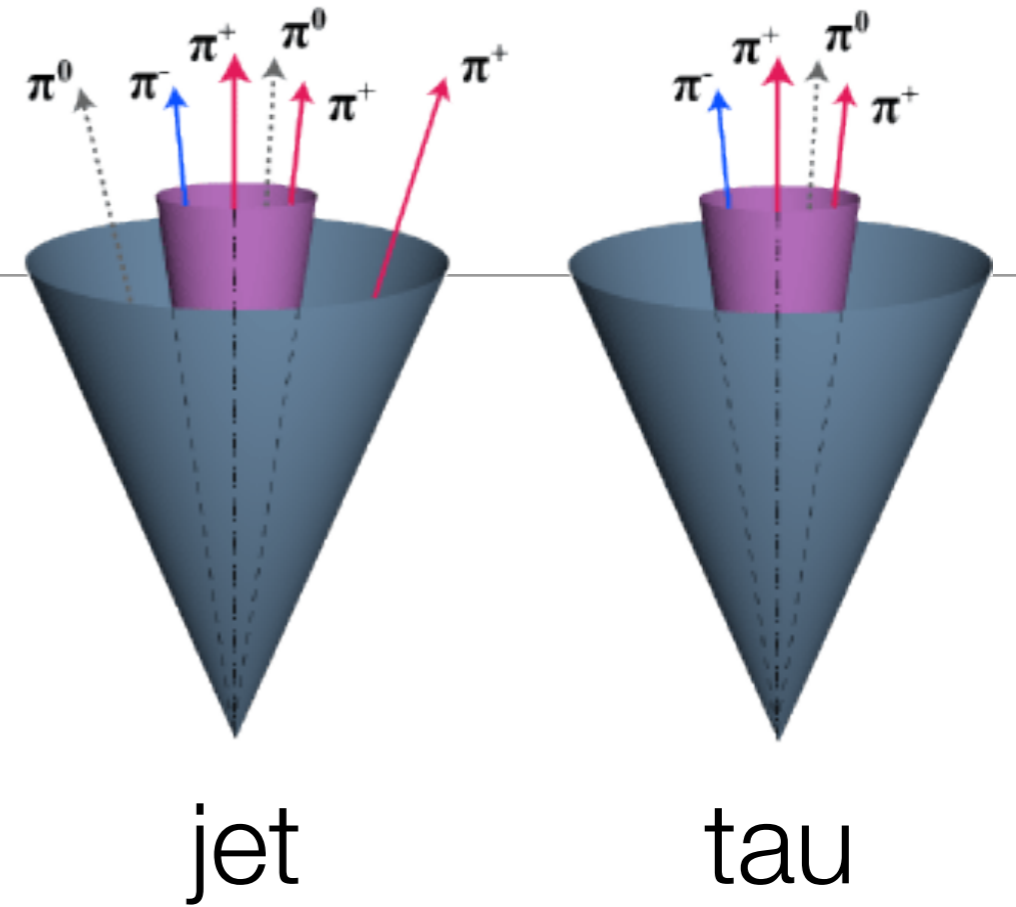
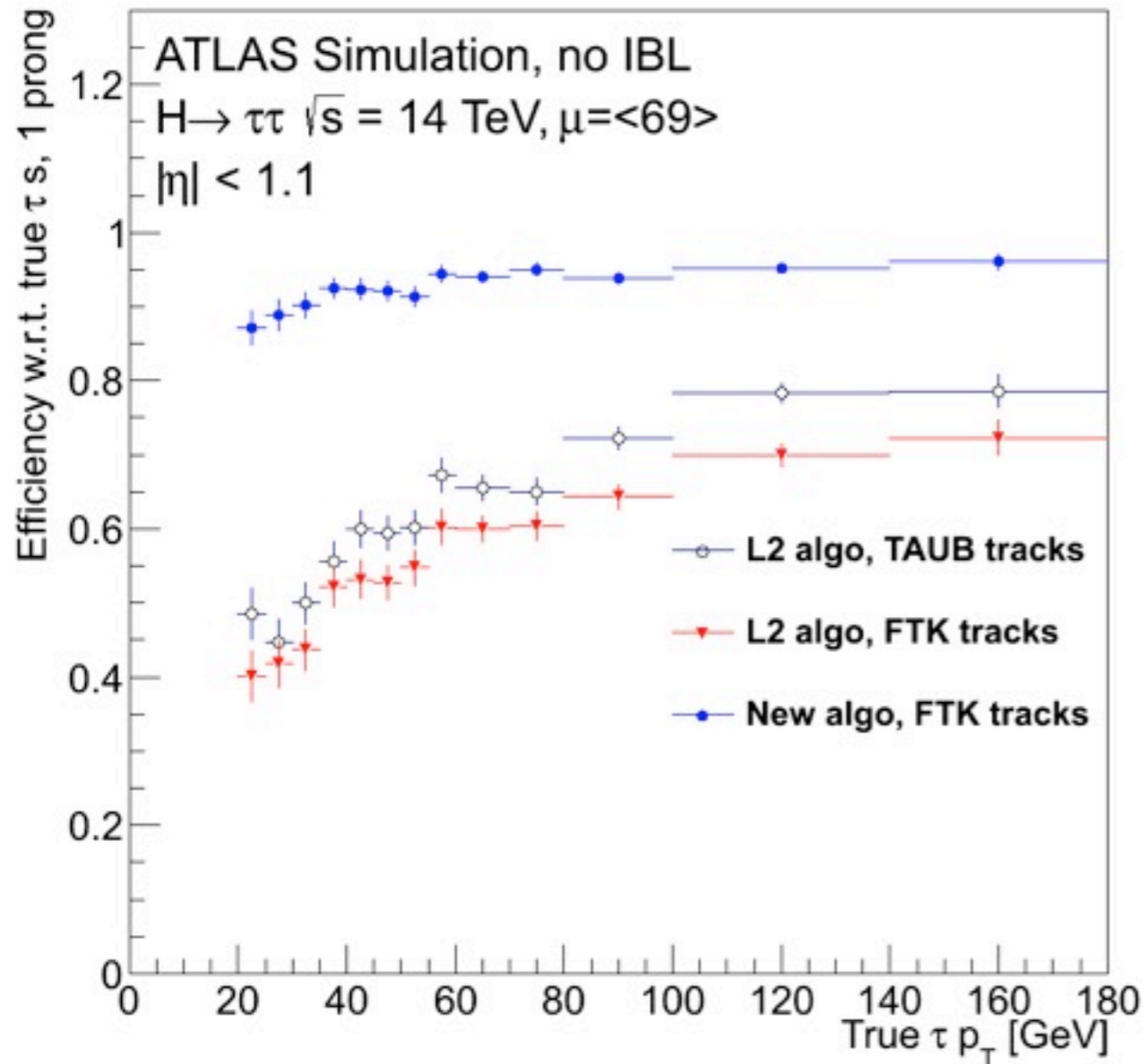
Performance: Taus



jet tau

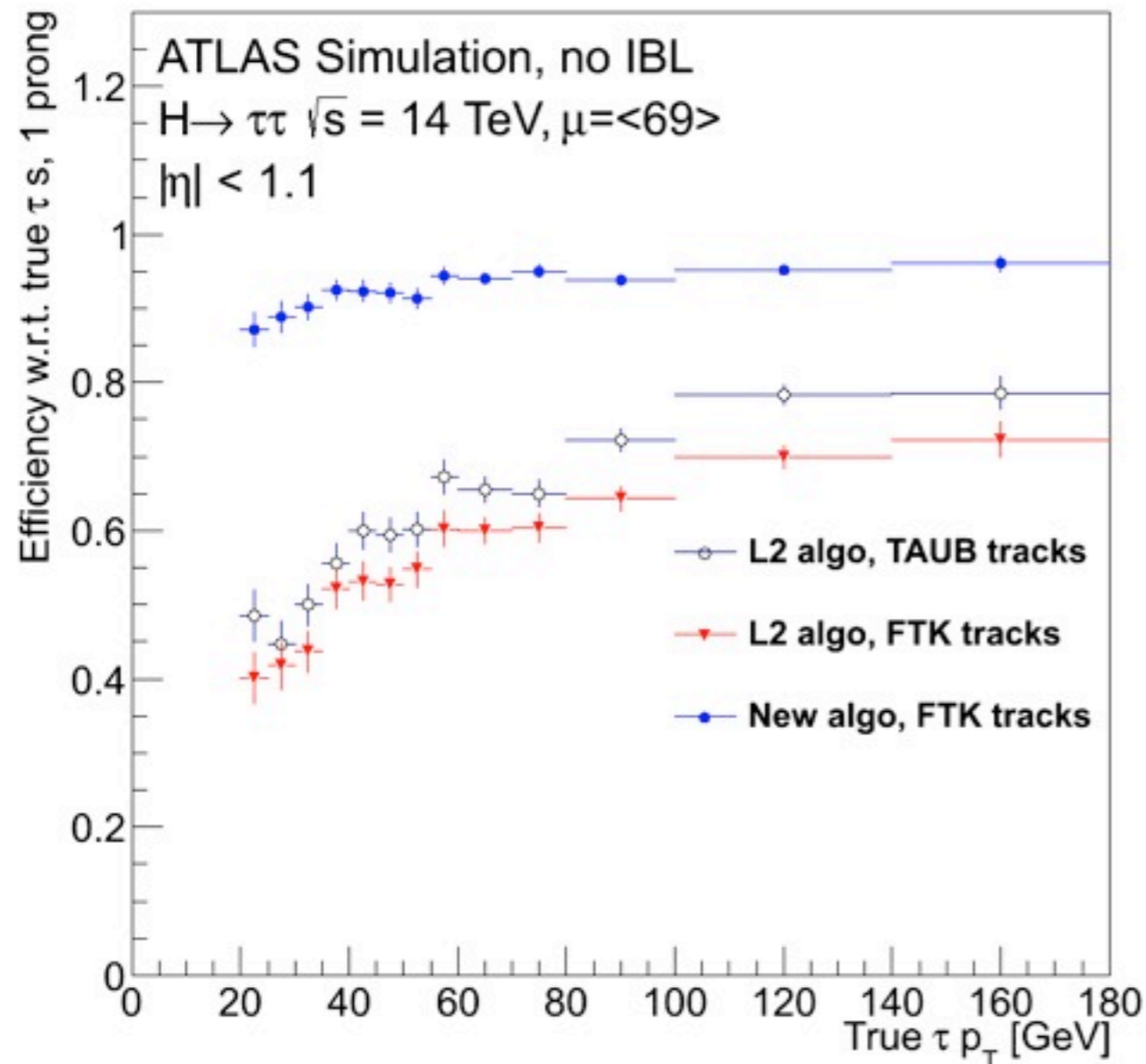
- Current tau algorithms run calo selection first, then tracking b/c of ROI tracking costs
- Replace L2 with simple track based selection
 - Then run more sophisticated calorimeter algorithms (not shown here)
 - Need to re-optimize offline in this case!

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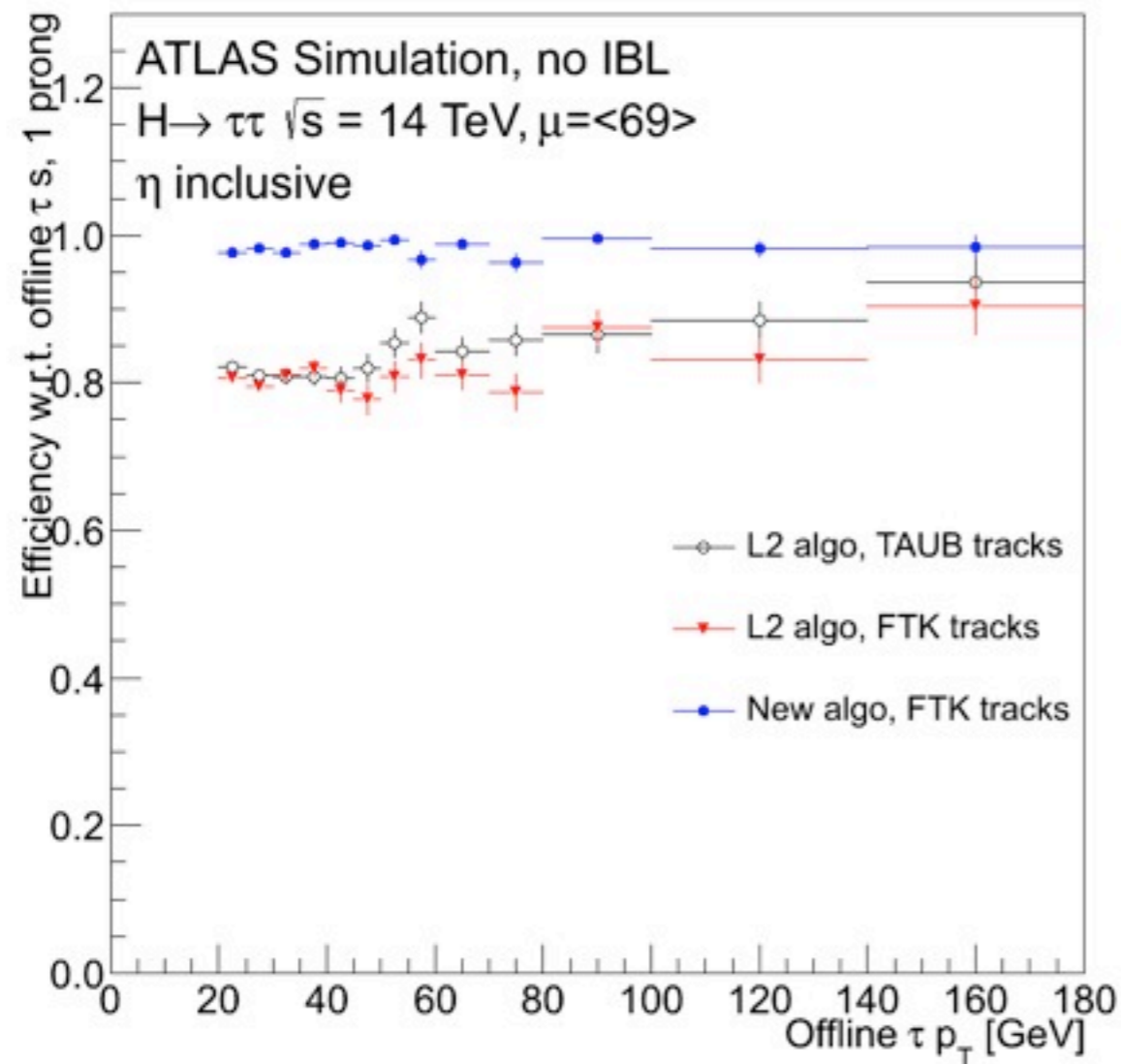
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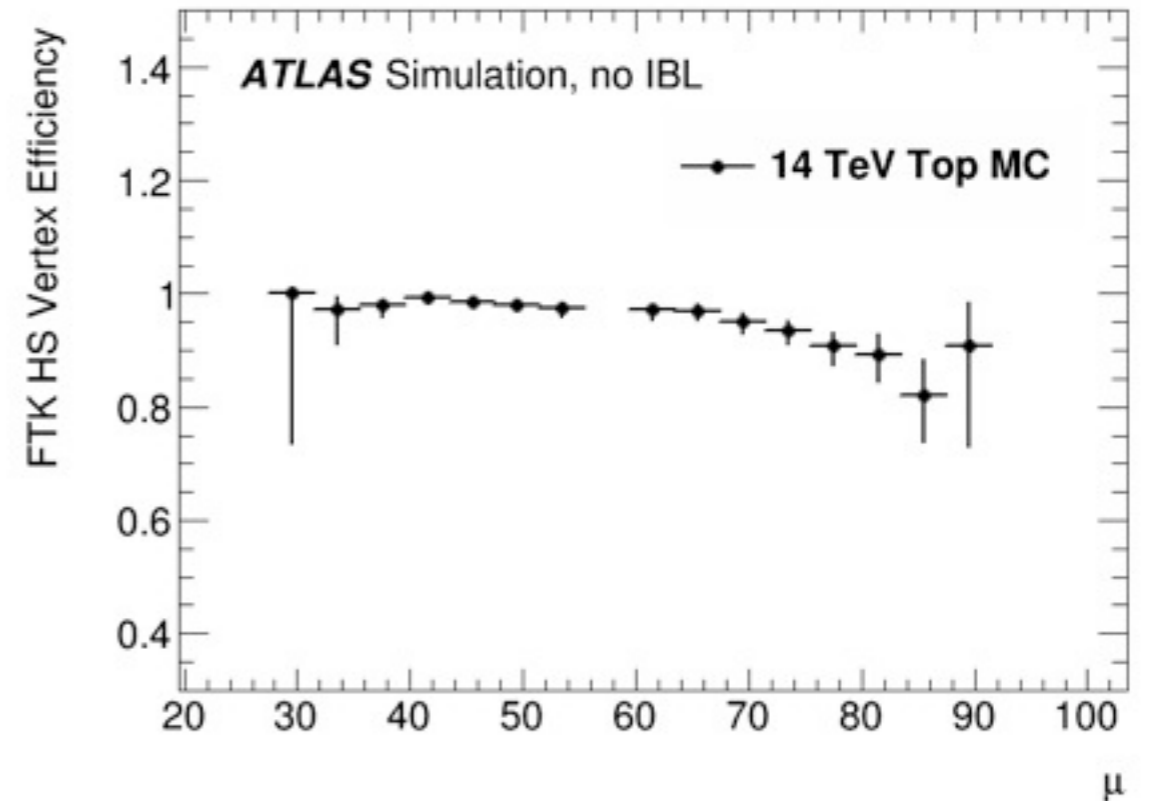
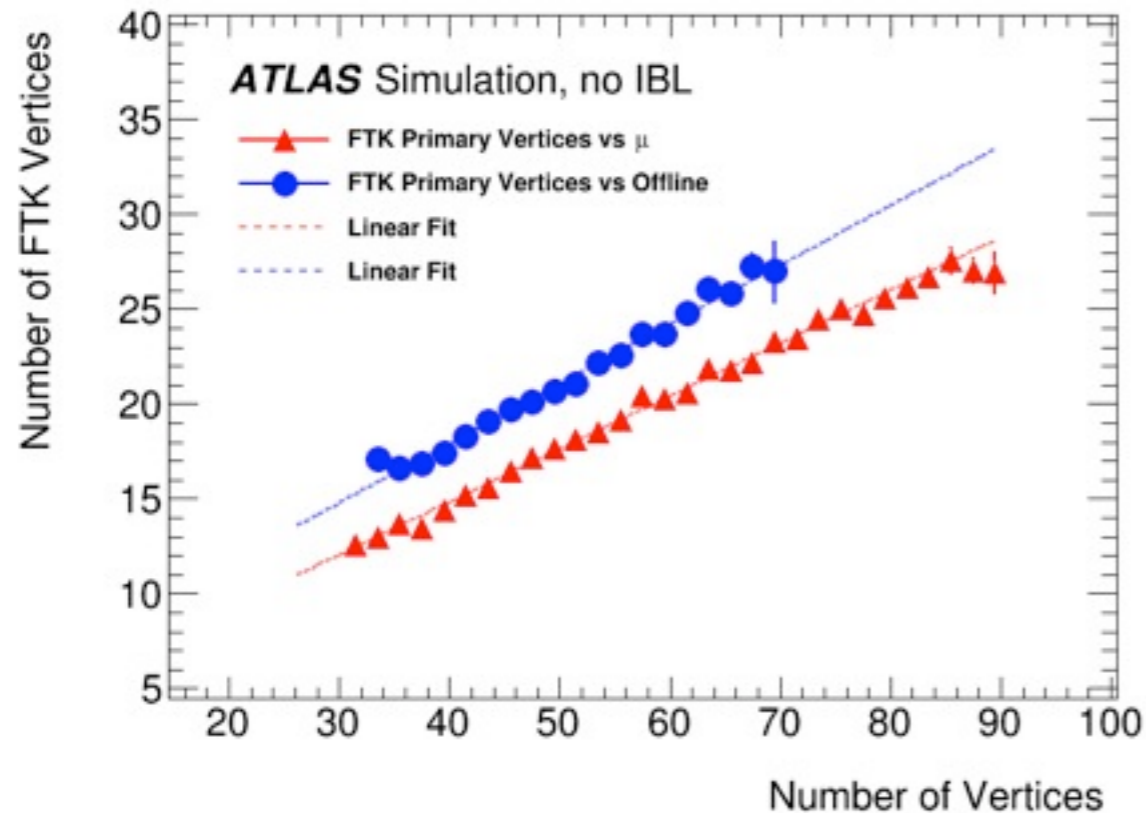
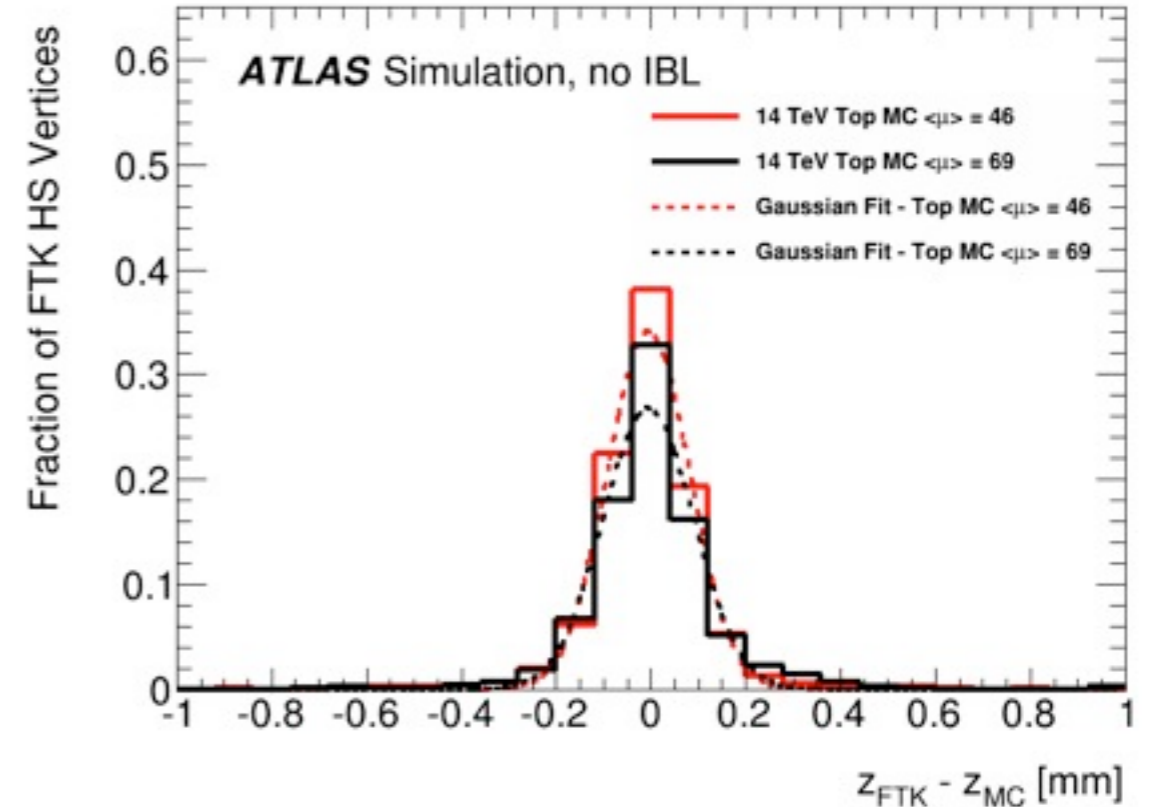


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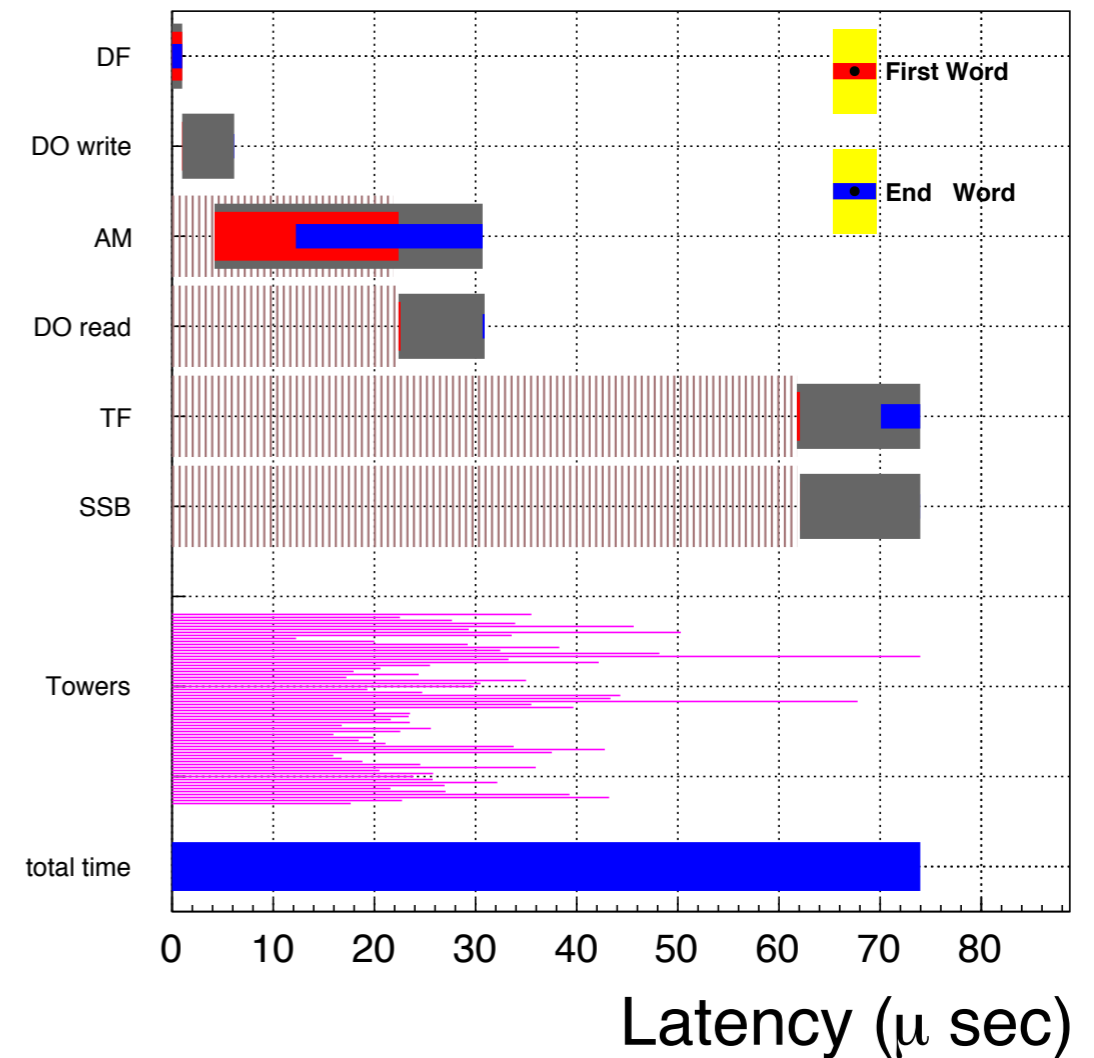
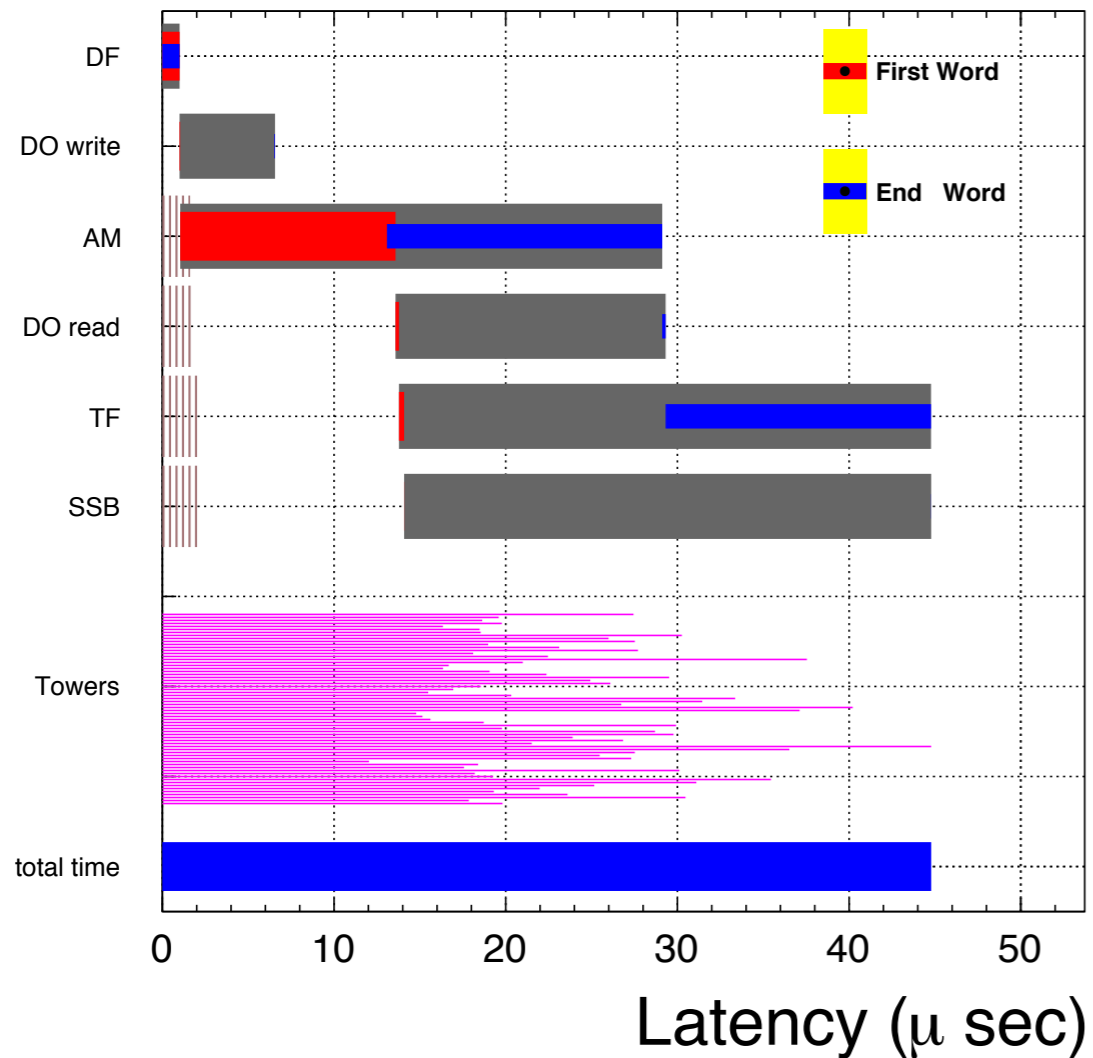
Performance: Primary Vertex Finding

- Can find PV with high efficiency with FTK tracks
 - Useful for multi-object association
- Can also do vertex counting
 - May need optimization to get better performance w.r.t offline



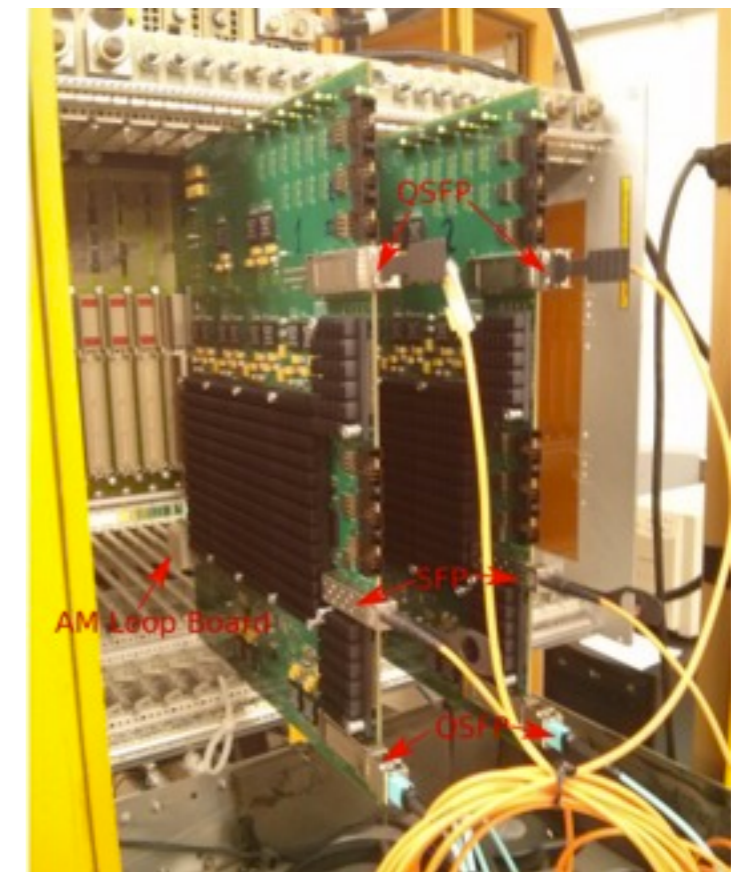
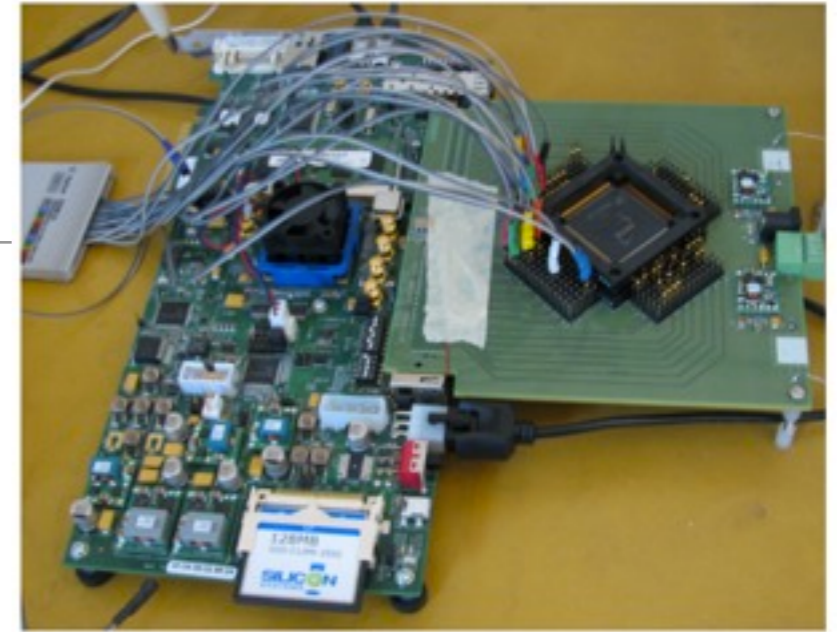
Timing Simulation

- Detailed timing studies based on per-word processing times for entire system
- 100 microsecond latency achievable at 70 interactions per crossing!

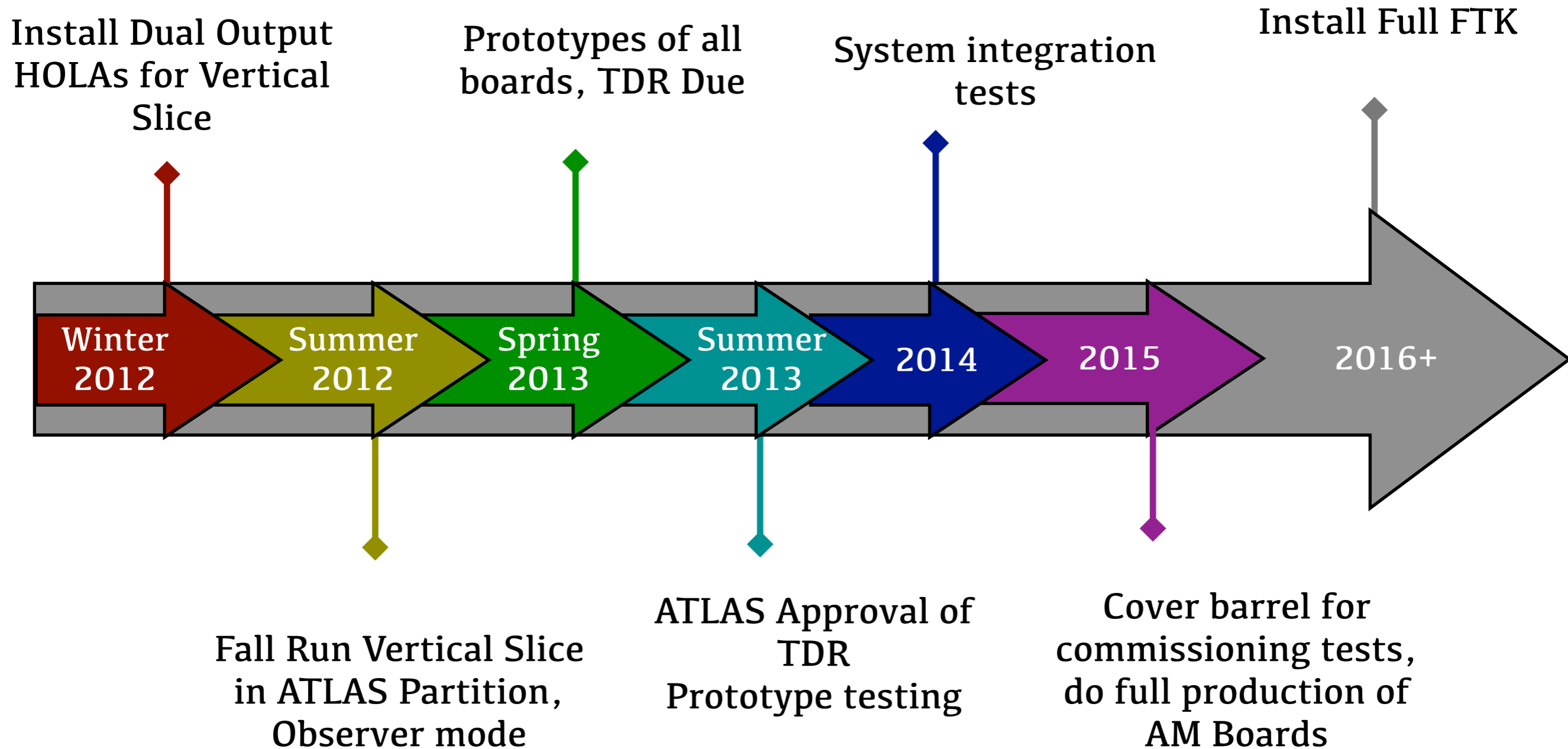


Summary of Prototype tests

- **AMChips: Custom cells tested and works well!**
- **Processing Unit:**
 - High speed communication between AUX and AMB successful
 - On board HS communication for AUX successful
 - Cooling tests for AMB underway to determine crate configuration
- **Clustering Mezzanine:**
 - Data transfer (SCT) tested in with collision data
 - Connection to DF through SMD connector tested
- **Data Formatter:**
 - Onboard and backplane data transfer tested to 10Gbps

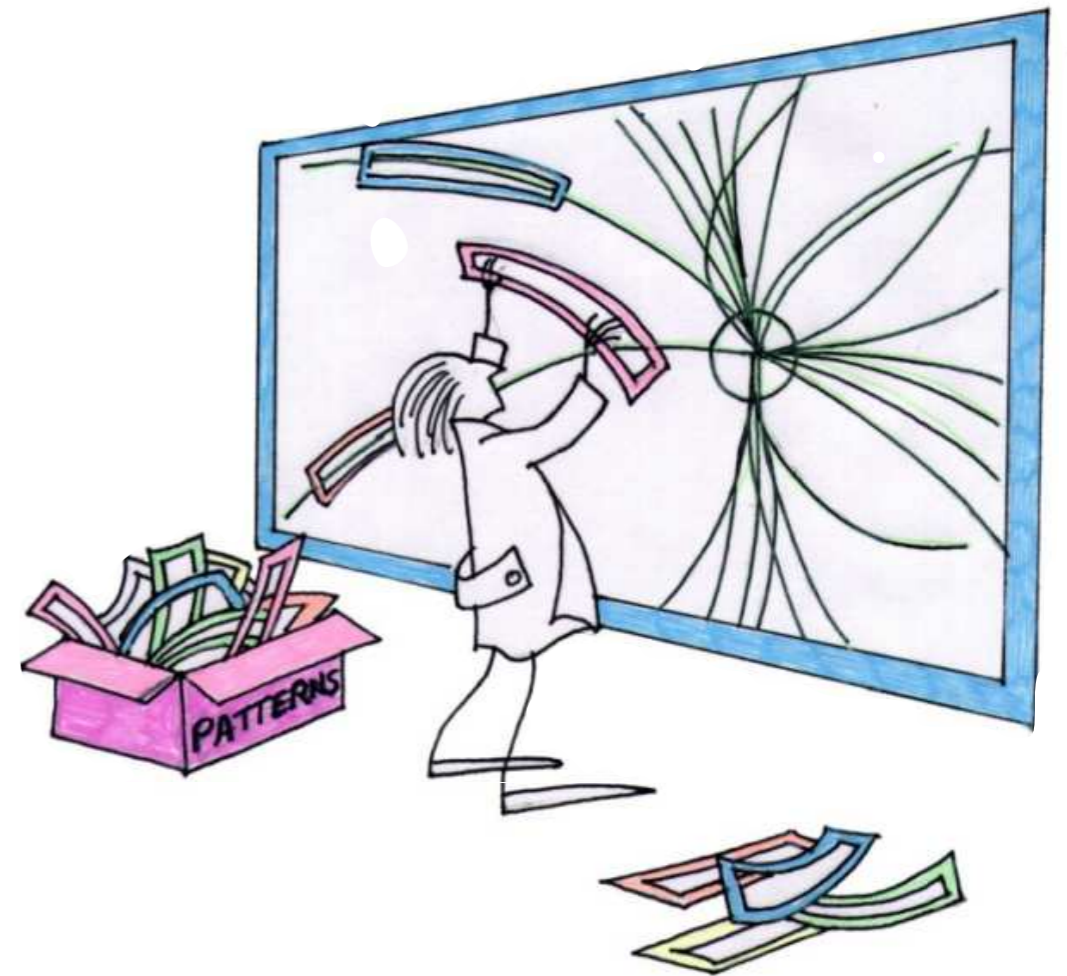


FTK Status and Plans



Conclusions

- LHC Run II & III will have a lot of challenging and exciting physics to be explored
 - Using tracking information in the trigger will increase our sensitivity to heavy flavor objects
- FTK uses a hardware solution to solve the problems of tracking at high luminosity
 - Good performance with respect to offline tracking
 - Trigger chains under development
- FTK is an approved ATLAS & LHCC project
 - All that remains is the Resource Review Board
- Installation begins in 2015, with full coverage most likely in 2016.



Back-up



THE UNIVERSITY OF
CHICAGO

LHC Plan*

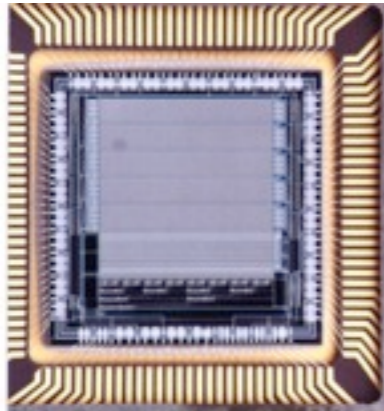
- Experiments request: 25 ns running with no significant 50ns dataset
- Machine reality: 50ns is easier/safer and will be used for 13 TeV commissioning before moving to 25 ns.
- Plan:
 - Low intensity for first 2 months, low number of bunches
 - Intensity ramp up with 50 ns (1-2months)
 - 50ns nominal running at $\langle \mu \rangle$ of 40 to characterize machine
 - 25ns commissioning
- May have to run at lumi-leveled 50ns operation if 25ns has problems
- Stable operations possibilities:

Scheme	N_b	ppb (10^{11})	β^* [cm]	emittance [μm]	peak	pile-up	\mathcal{L} [fb^{-1}]
25 ns	2760	1.15	55/43/189	3.75	9.3e33	25	24
25 ns BCMS	2760	1.15	45/43/189	1.9	1.7e34	52	45
50 ns	1380	1.65	42/43/189	2.3	1.6e34	87	40 [†]
50 ns BCMS	1380	1.6	38/43/189	1.6	2.3e34	138	40 [†]



AM technological evolution

SVT
AM chip



- (90's) **Full custom VLSI chip** - $0.7\mu\text{m}$ (INFN-Pisa)
- **128 patterns, 6x12bit words each, 30MHz**
F. Morsani et al., IEEE Trans. on Nucl. Sci., vol. 39 (1992)

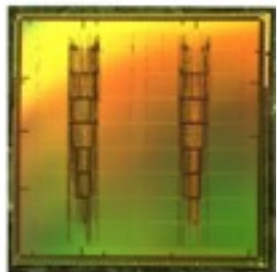
Alternative **FPGA** implementation of SVT AM chip

P. Giannetti et al., Nucl. Instr. and Meth., vol. A413/2-3, (1998)

G Magazzù, 1st std cell project presented @ LHCC (1999)



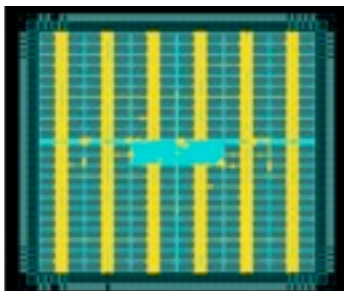
SVT upgrade



Standard Cell $0.18\ \mu\text{m}$ \rightarrow 5000 pattern/AM chip

SVT upgrade total: 6M pattern, 40MHz
A. Annovi et al., **IEEE TNS**, Vol 53, Issue 4, Part 2, 2006

FTK R&D



AMchip04 –65nm technology, std cell & full custom, 100MHz
Power/pattern/MHz \sim 30 times less. Pattern density x12.

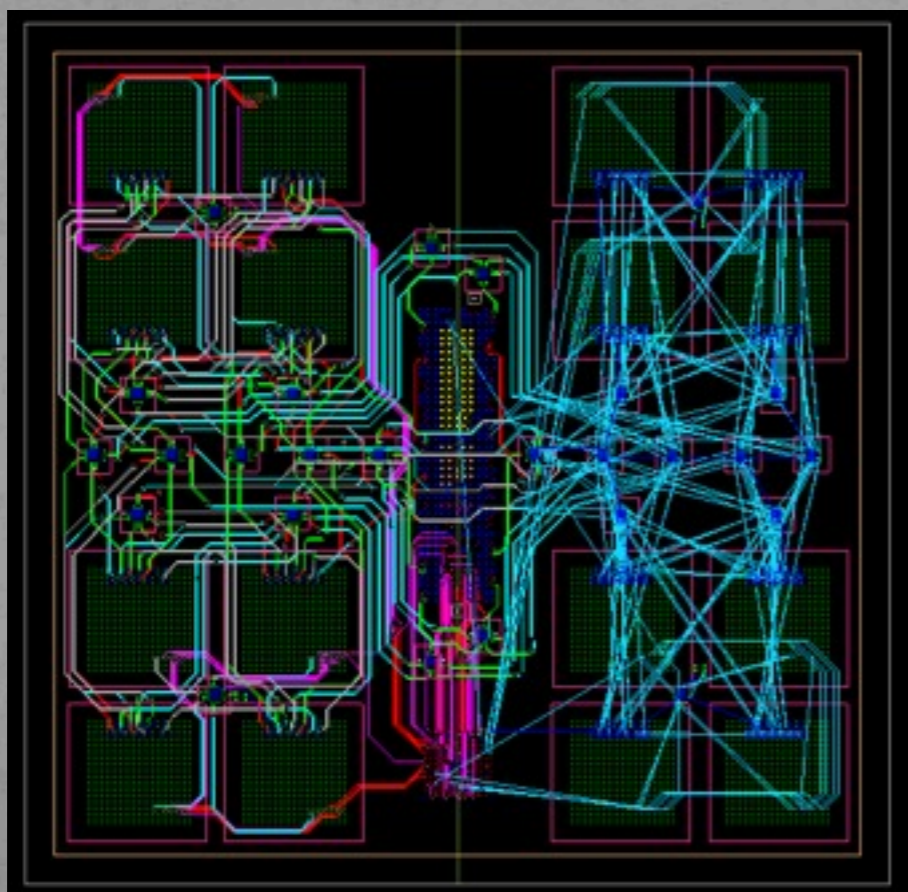
First variable resolution implementation!

F. Alberti et al 2013 *JINST* 8 C01040, doi:10.1088/1748-0221/8/01/C01040

The Clustering Implementation

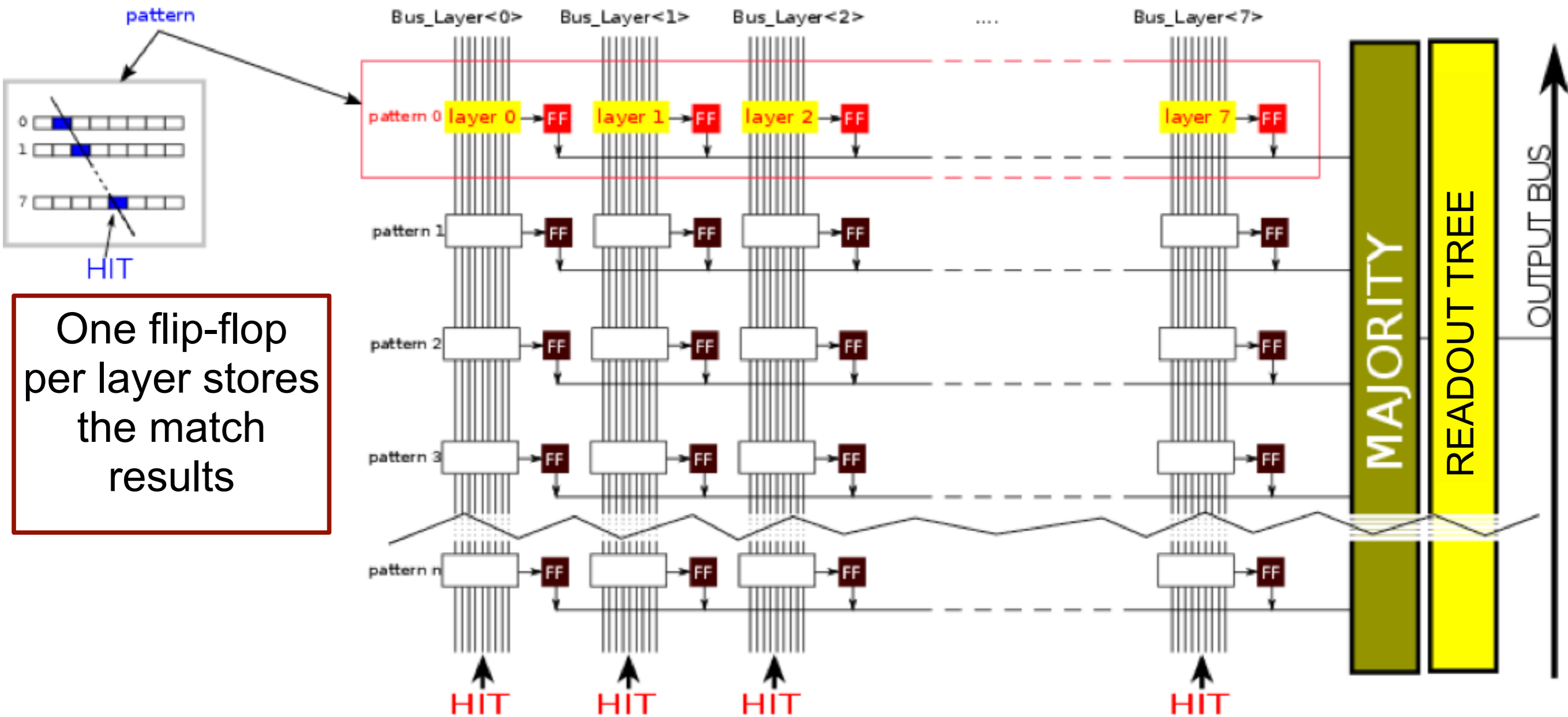
- The current implementation is an evolution of a linear algorithm with a high cost in terms of FPGA resources
- In the previous algorithm grids of 168x4 or 328x8 pixels were used. For these grid sizes the extrapolated area and clock results (for the Spartan 6-LX150T) would be:

Grid Size	Slice Registers	Slice LUTs	Clock	Frequency
21x8 (current)	696 (1%)	1950 (2%)	12ns	83Mhz
168x4	2784 (1.5%)	7800 (8.2%)	68ns	14.8Mhz
328x8	10510 (5.7%)	30457 (33%)	265ns	3.8Mhz

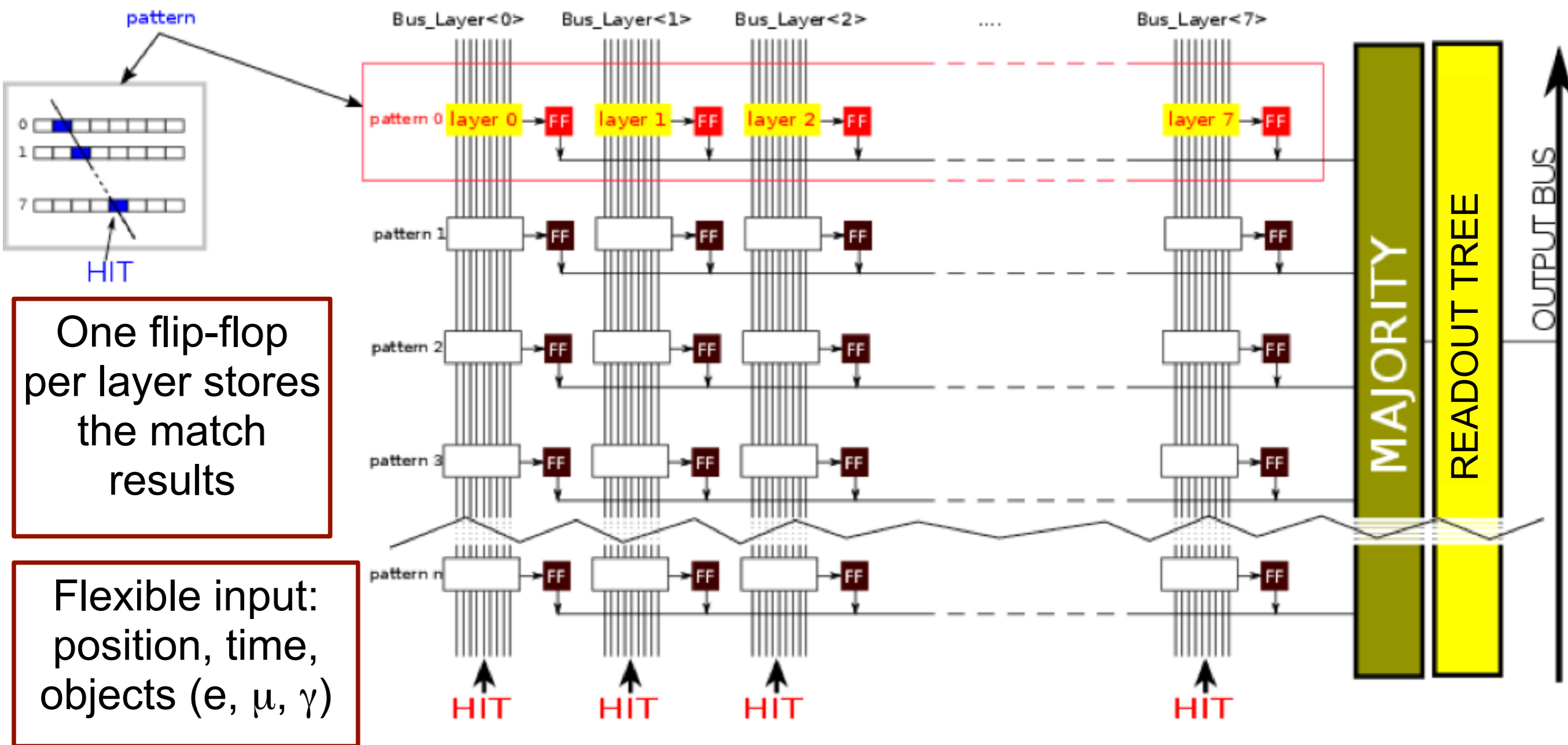


- AMBFTK is EURCARD 9U format
- Massive serial I/O
 - 2 Artix 7 FPGAs
 - Only serial communication busses
- Additional FPGAs for VME control
 - Slave for VME communication in the AUX-card
- LAMB redesigned for the newer AM-chip
 - Serial communication replaced the parallel busses
 - See M. Beretta talk on 24/09
 - <https://indico.cern.ch/contributionDisplay.py?contribId=50&confId=228972>
- Different voltages to be distributed
 - 3.3V for the I/O
 - 1.2V AM-chip
- High power consumption, about 200 W

AM working principle

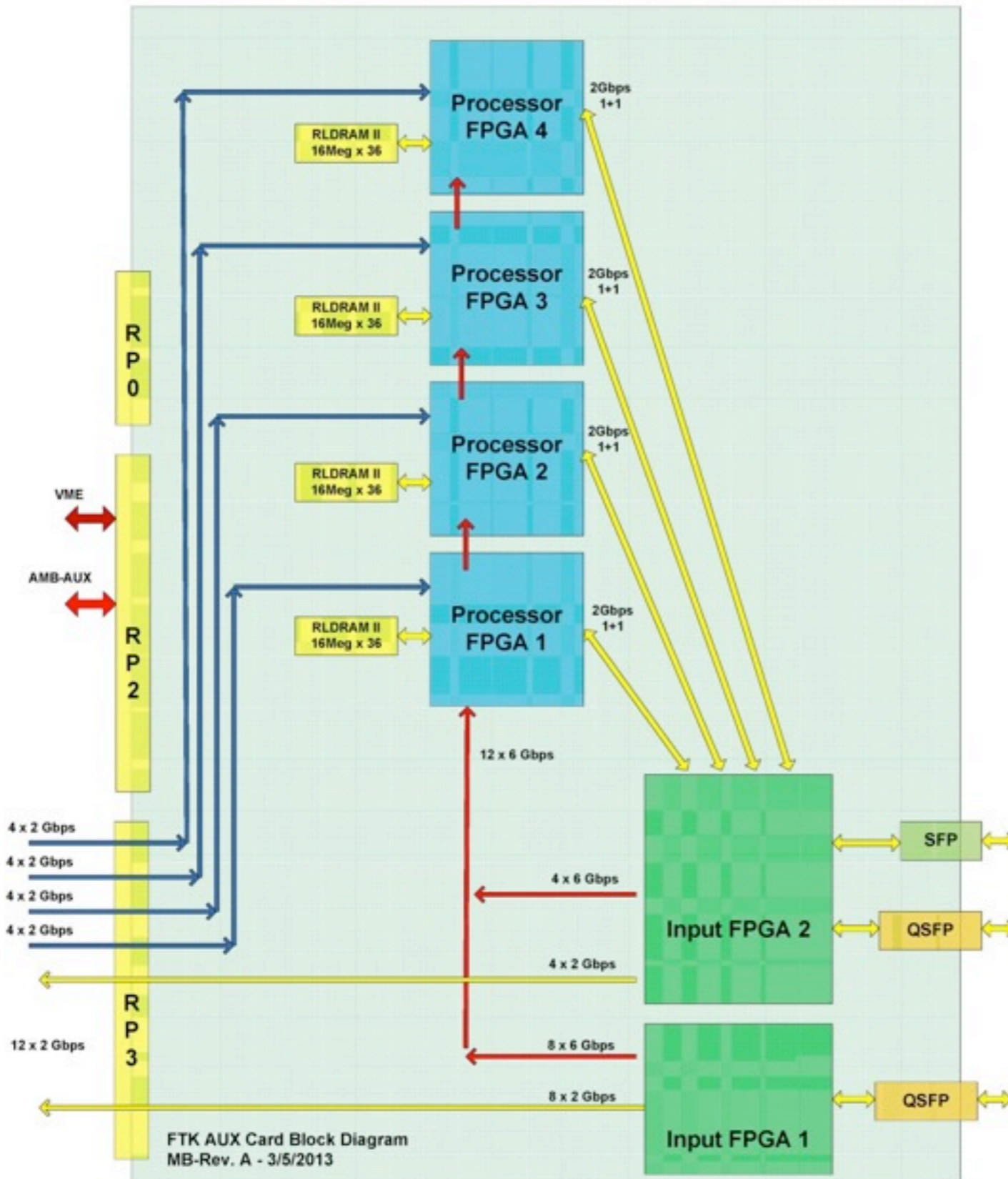


AM working principle



Pattern matching is completed as soon as all hits are loaded.
Data arriving at different times is compared in parallel with all patterns.
Unique to AM chip: look for correlation of data received at different times.

AUX



- 9U VME Rear Transition Card
 - 280mm deep!
- I/Os:
 - Fibers: to DF, SSB
 - 2 x QSFP (8 x RxTx @ 6Gbps)
 - 1 x SFP (1 x RxTx @ 2Gbps)
 - P3 Connector: Data to AMB
 - 12 x Out @ 2Gbps
 - 16 x In @ 2Gbps
 - P2 Connector: VME control, power
- Processing power: 6 Arria V FPGAs
 - 20 Mb RAM, ~1000 DSPs each